



Contribution ID: 99

Type: Oral Presentation

## Trigger and Data Acquisition systems readout architecture of the Tile PreProcessor Demonstrator for the ATLAS Tile Calorimeter phase-II upgrades.

*Tuesday, 4 July 2017 14:20 (20 minutes)*

The LHC has planned a series of upgrades culminating in the High Luminosity LHC (HL-LHC) which will have an average luminosity 5-7 times larger than the nominal Run-2 value. The ATLAS Tile Calorimeter (TileCal) will undergo an upgrade (phase-II) to accommodate the HL-LHC parameters. The TileCal both on and off-detector electronics will be completely redesigned and a new Trigger and Data Acquisition (TDAQ) system readout architecture will be adopted for this upgrades. With this new readout strategy, the front-end electronics will transmit readout data for every bunch crossing (25 ns) to the first element of the back-end electronics viz. the Tile PreProcessors (TilePPr). The TilePPr is a high-performance double AMC board based on FPGA resources and QSFP modules. This board has been designed in the framework of the ATLAS TileCal Demonstrator project for the phase-II upgrades as the first stage for the back-end electronics. The TilePPr will provide an interface path for the readout, configuration, control and monitoring of the front-end electronics, and will send calibrated information to the ATLAS Level 0 trigger system for trigger decision. A single TileCal drawer module commissioned with the phase-II upgrade electronics is to be inserted into the real detector to evaluate and qualify the new readout and trigger concepts in the overall ATLAS TDAQ system. This new drawer, so-called Hybrid Demonstrator, must provide an analog trigger signal for backward compatibility with the current system. This Demonstrator drawer has been inserted into a TileCal module prototype to evaluate the performance in the lab. In parallel, one more TileCal module has been instrumented with two other front-end electronics options based on custom ASICs (QIE and FATALIC) which are under evaluation. These two modules equipped with the Phase-II upgrade electronics together with three other modules instrumented with the current system electronics were exposed to different particles and energies in three test-beam campaigns during 2015 and 2016. This contribution will describe in detail the various components of the TDAQ infrastructure of the upgrade specific electronics, and some preliminary results from the test beam campaigns.

**Apply to be considered for a student award (Yes / No)?**

Yes

**Level for award (Hons, MSc, PhD, N/A)?**

MSc

**Main supervisor (name and email) and his / her institution**

Prof. Bruce Mellado  
 Bruce.Mellado@wits.ac.za  
 University of the Witwatersrand

**Would you like to <br> submit a short paper <br> for the Conference <br> Proceedings (Yes / No)?**

Yes

**Primary author:** Mr HLALUKU, Dingane (Student)

**Co-authors:** Dr VALERO, Alberto (Instituto de Fisica Corpuscular (UV-CSIC)); Mr CARRIO, Fernando (University of Valencia / CERN)

**Presenter:** Mr HLALUKU, Dingane (Student)

**Session Classification:** Applied Physics

**Track Classification:** Track F - Applied Physics