TDAQ systems readout architecture of the Tile Preprocessor Demonstrator for the ATLAS Tile Calorimeter phase-II upgrades

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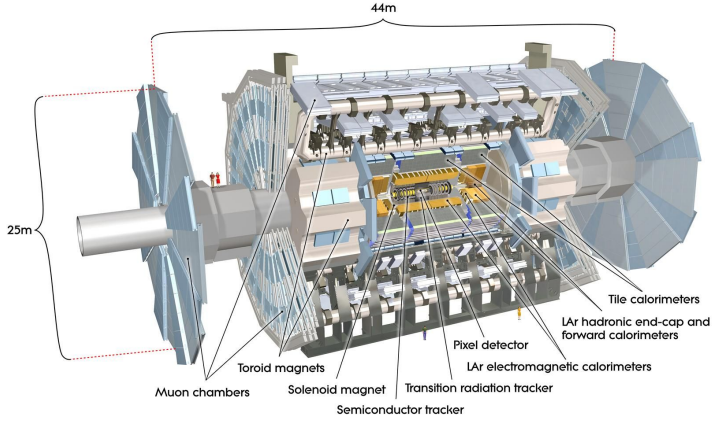
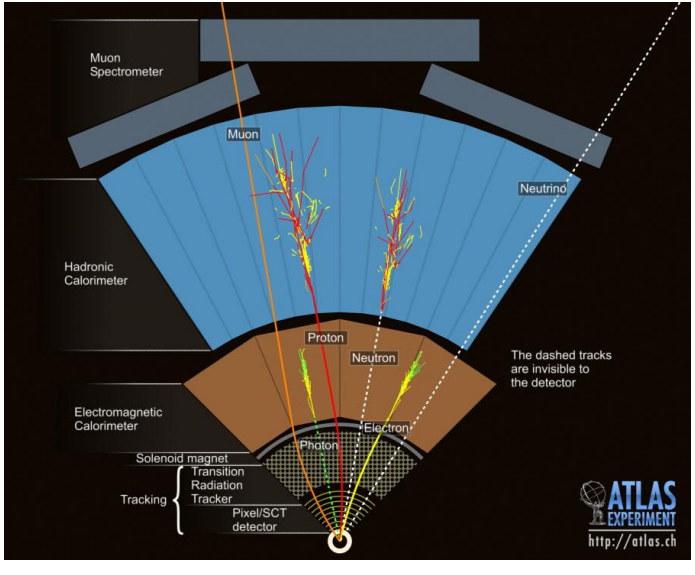
OVERVIEW

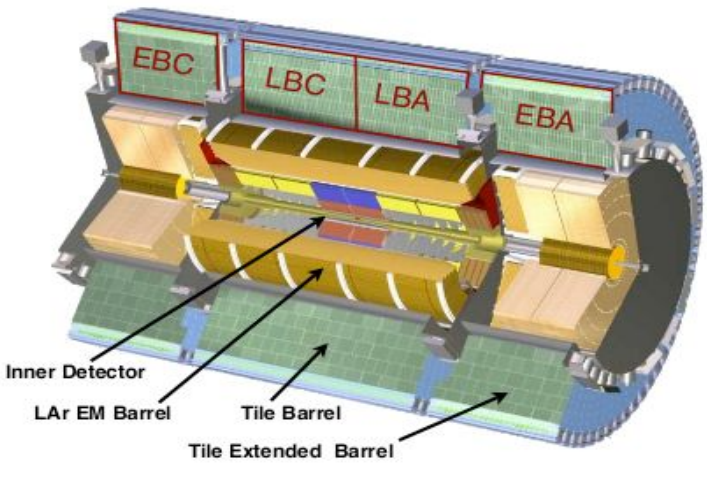
- Introduction
  - Tile Calorimeter
- Trigger and Data AcQuisition (TDAQ) overview and terminology
- TileCal upgrades
- Tile PreProcessor for phase-II
- Demonstrator project
  - Options and changes
- Test with beam setup campaigns
- PPr TDAQ software
- Tests with FELIX
- Test with beam setup results
- Conclusions



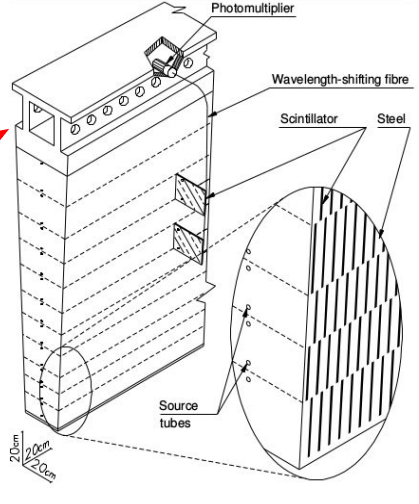


INTRODUCTION: TILE CALORIMETER

- The hadronic Tile Calorimeter (TileCal) is the central region of the ATLAS detector and is used to measure energies and directions of hadrons, jets and leptons.
- It is a large sampling calorimeter which makes use of steel as the absorber material and plastic scintillating plates readout by Photomultipliers Tubes (PMTs) through wavelength shifting (WLS) fibers.
- Mechanically divided into three barrels, one central barrel and two extended barrels.
- And operationally, the system is split into four logical partitions which are labeled as LBA and LBC for the long barrel, and EBA and EBC for the extended barrel.
- Signals and data from the detector is processed by the Trigger and Data Acquisition (T/DAQ) system.



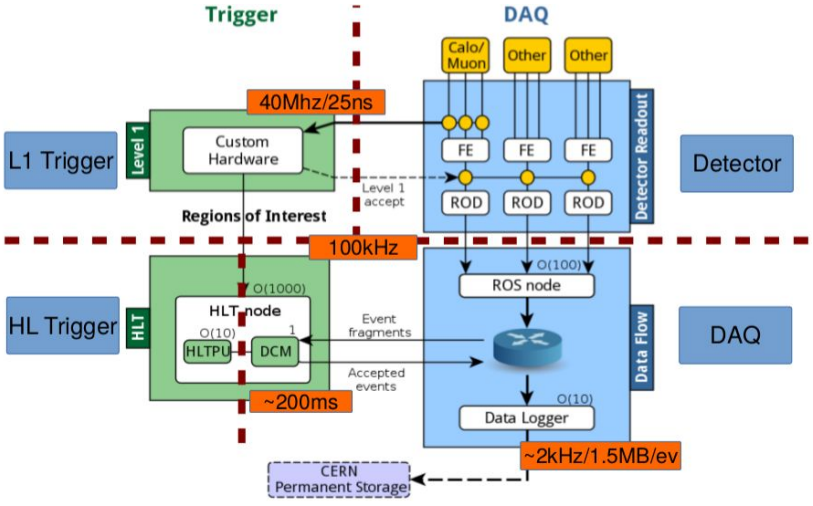
ATLAS Calorimeter system



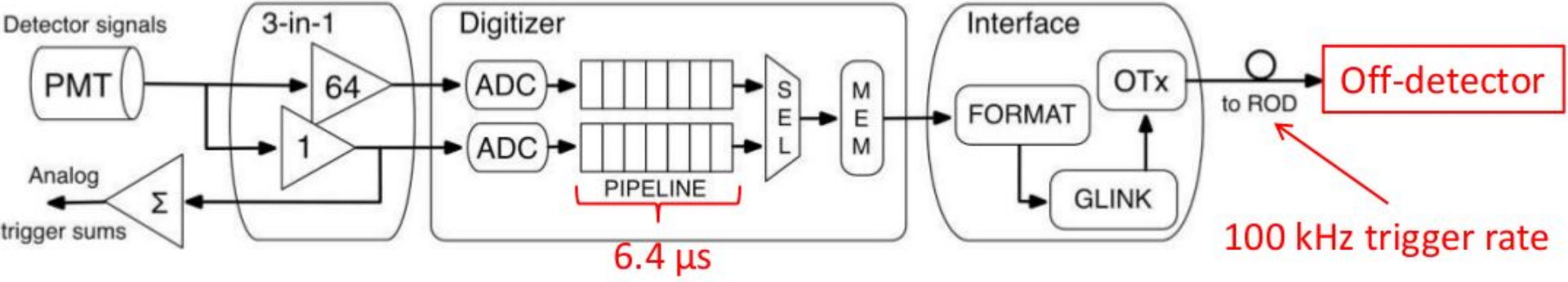
TileCal Module

T/DAQ OVERVIEW & TERMINOLOGY

- Trigger: Selects interesting events in real time.
  - Level-1: hardware based, rejection factor ~400.
  - High-Level Trigger: software based, rejection factor ~100.
- DAQ: Collection of apps (~30k) running on set a set of hosts.
  - Receives event fragments and buffer them in pipelines.
  - Readout fragments through ROS and feed HL trigger.
  - Build complete events and write event data to disk.
  - Provide control, configuration and monitoring facilities.
- Particles from collisions travel through the TileCal deposit energy in the scintillating tiles which produces light, the light is collected by the PMTs through the WLS fibers.
- The current TileCal T/DAQ architecture readout electronics will be completely redesigned for HL-LHC phase-II upgrades.



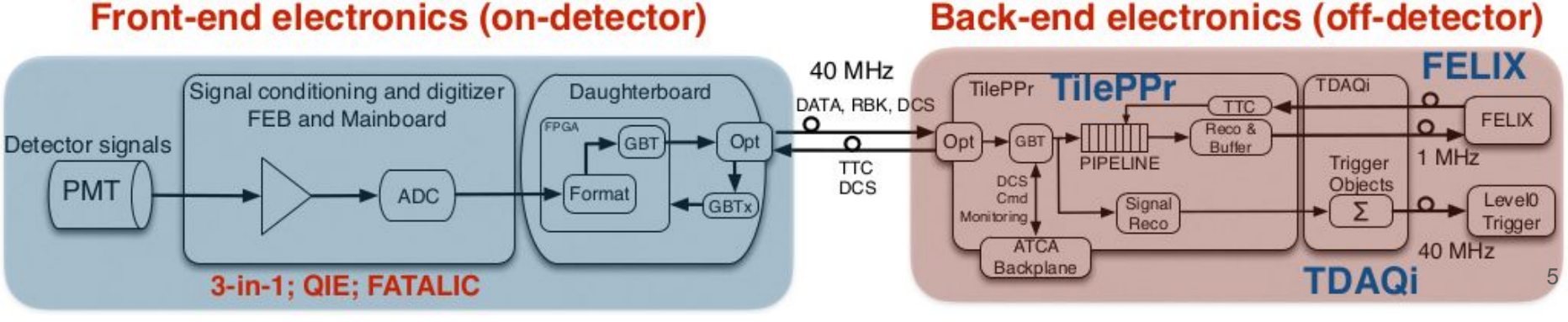
ATLAS T/DAQ system



TileCal current T/DAQ architecture

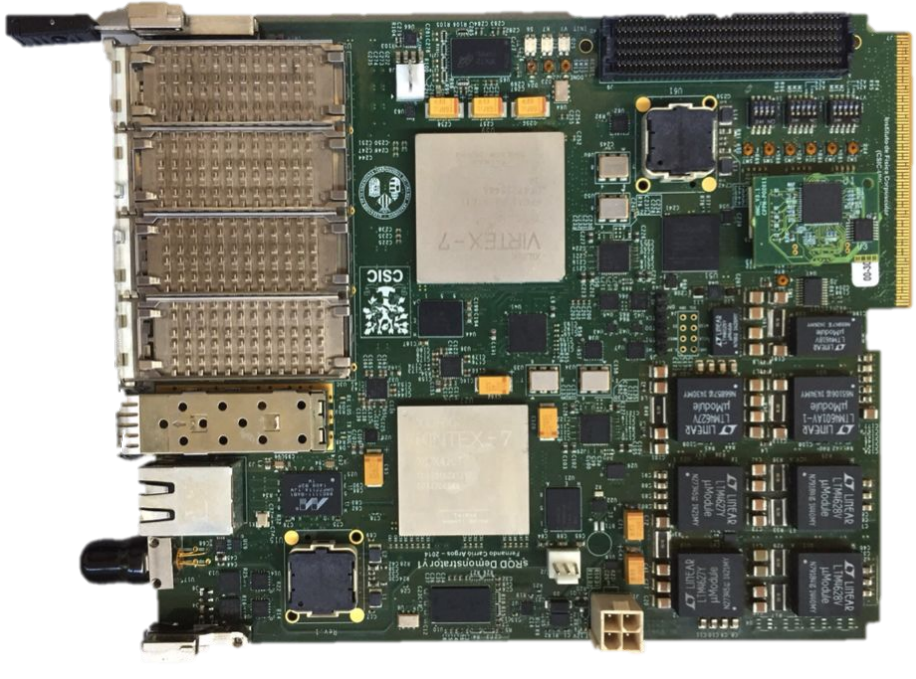
TILECAL UPGRADES

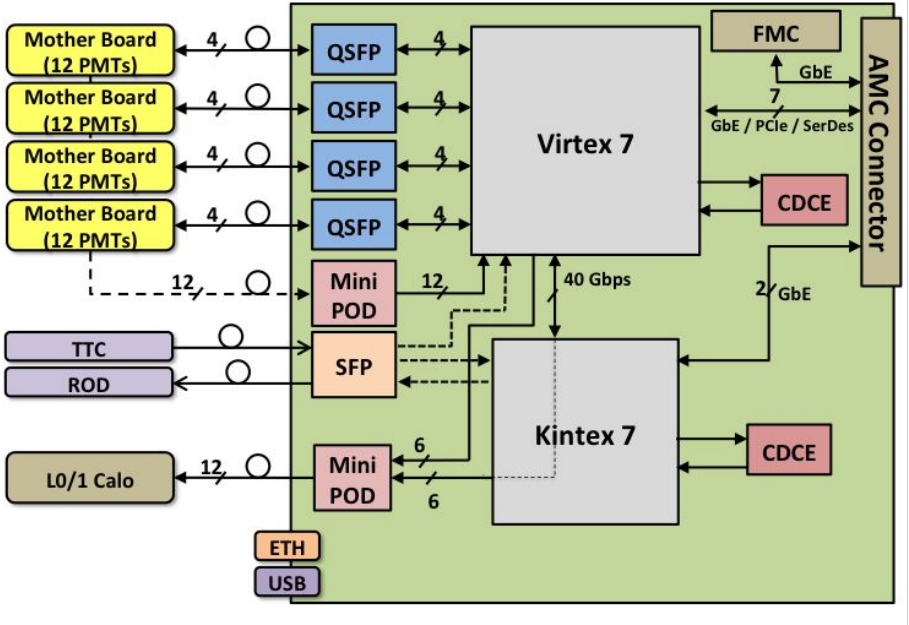
- The LHC plans a series of upgrades culminating in the High Luminosity (HL-LHC) in order to reach its intended design luminosity of 7.5 x 10^{34} cm^{-2} s^{-1} in 2023.
  - A new readout architecture with a full-digital trigger system will be implemented in ATLAS for Phase II Upgrade to cope with the new requirements. TileCal will undergo upgrades as well to cope with the HL-LHC.
  - The detector components (scintillating tiles, fibers, and PMTs) are in good shape and do not have to be replaced.
- The readout electronics has to be replaced since present digital readout is not compatible with the HL-LHC architecture.
  - Aging of parts (time & radiation). Some parts are discontinued.
  - To provide full-granularity digital data to the Level-0/1 triggers at 40 MHz.
  - The present on-detector electronics is designed to output digital data at the maximum rate of about 100 kHz.
  - The digital data is stored on detector in a 6.4 μs-long pipeline.
- In the new TDAQ architecture, the front-end (FE) electronics will transmit data to the back-end (BE) electronics Tile PreProcessor (PPr) for every bunch crossing (25 ns) and stored in pipelines for processing.
- The new FE electronics are much simpler and will not have any readout limitations like the present system.



THE TILE PPr FOR PHASE-II UPGRADES

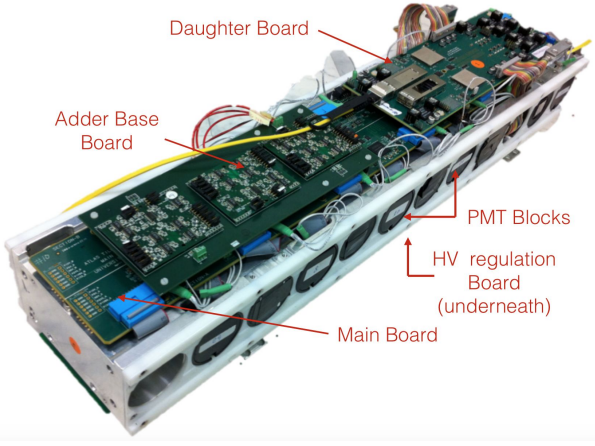
- Is a high performance double AMC board based on FPGA resources and QSFP modules.
- This board has been designed in the ATLAS TileCal Demonstrator project as the first stage for the BE electronics.
- It provides an interface path for readout, control and monitoring of the FE electronics, and sends Level 0/1 info to ATLAS for trigger decision.
- Decodes and distributes Trigger Timing and Control (TTC) signals to the FE electronics for configuration and synchronization with the LHC clock.
- First prototypes manufactured by the Wits High Energy Physics group in South Africa.



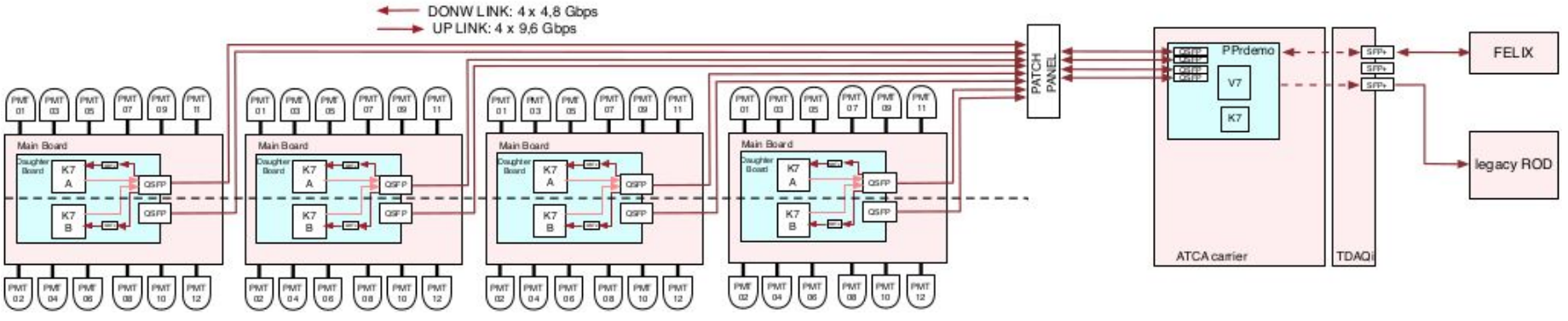


THE TILECAL DEMONSTRATOR PROJECT

- Aims to validate on the new T/DAQ architecture system interfaces before the complete installation of the upgraded electronics in ATLAS.
- Super-drawer DEMONSTRATOR composed of 4 independent mini-drawers;
  - 12 PMTs, 12 FE boards (FEB), 1 of 3 options.
  - 1 MainBoard (MB): for the corresponding FEB option and ADC chips.
  - 1 Daughter-board (DB): common design.
  - 1 High Voltage regulation board: 2 options (Remote HV & HV_Optos).
  - 1 adder base board + 3 adder cards (for trigger).
  - New Low Voltage Power Supply (LVPS) architecture : redundancy and Point Of Load regulators - LVPS v.8.01.
- Upgrade readout strategy;
  - Data is readout at 40 MHz to the Demonstrator PPr.
  - Digital trigger with possible full granularity and precision.
  - Read-out to Front End LInk eXchange (FELIX) after L0 or L1.

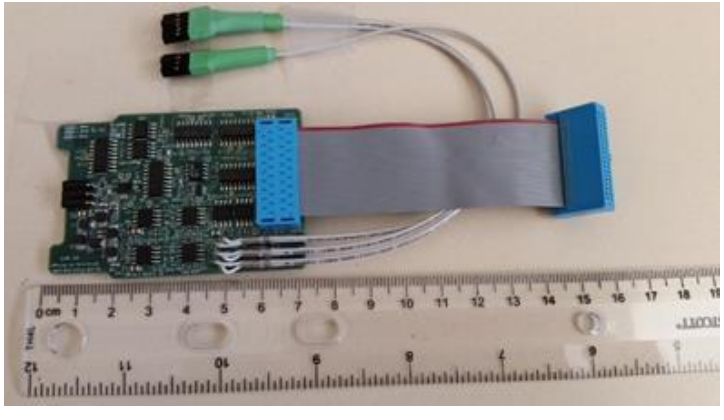


Max PMT# in a detector drawer is 45, even though the Mainboard can load up to 48 PMTs.

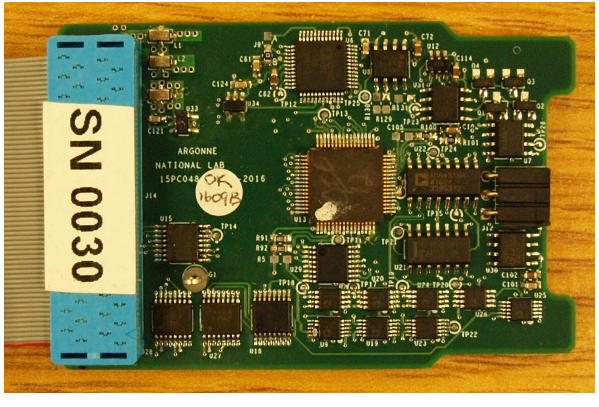


THE TILECAL DEMONSTRATOR PROJECT

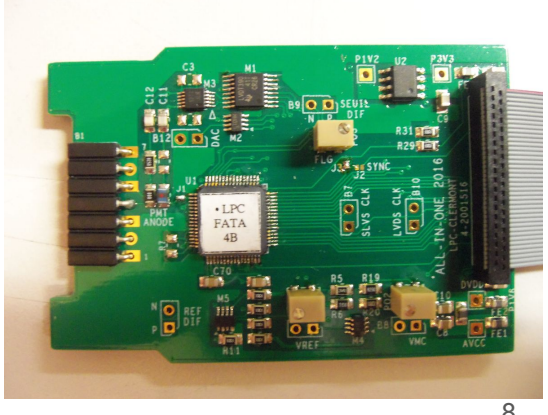
- A series of tests with beam setup have been initiated in 2015 and are on going with the following objectives:
  - Aiming at the physics measurements (electrons, muons and hadrons).
  - Assess the status of the demonstrator prototype based on the 3-in-1 FEB baseline option and the BE PPr.
  - Attention to FATALIC and QIE, and estimate future commission efforts.
  - Measuring some detector performance in a well controlled environment for ATLAS.
- The FEB options under evaluation for phase-II are the:
  - **3-in-1** option. Design following the same approach presently used in TileCal with improved performance from experience learned. Sharper, bi-gain clamping amplifiers and slow integrator 12b ADCs on MB.
  - **Charge Integrator and Encoder (QIE)**. New technology for TileCal, but used in other experiments(e.g. CMS). It is an ASIC that does signal conditioning by means of an integrator.
  - **Front-End ATLAS Tile Integrated Circuit (FATALIC).** New technology for TileCal implemented as an ASIC aiming for a low noise chip. FATALIC does signal conditioning by means of a shaper (similarly to 3-in-1).
- All 3 options have been evaluated in the lab during test beam campaigns in 2015, 2016 and 2017.



3-in-1 FEB



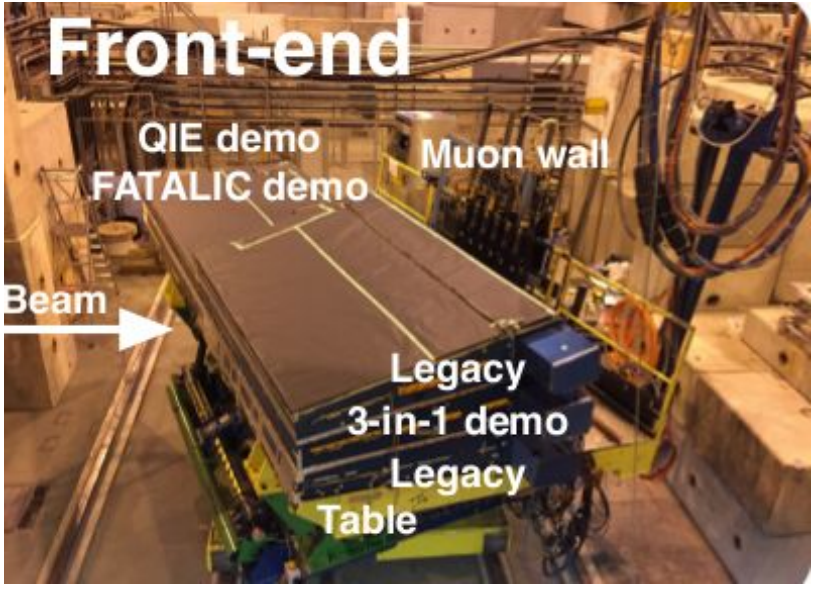
QIE FEB



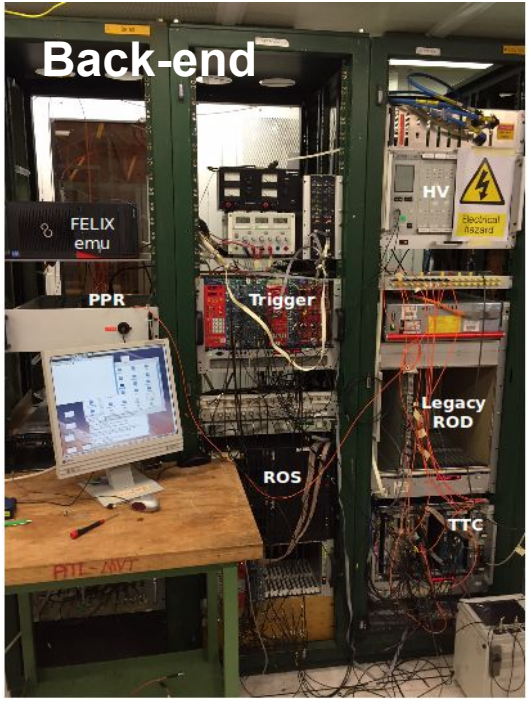
FATALIC FEB

TEST WITH BEAM SETUP CONFIGURATION

Beam elements



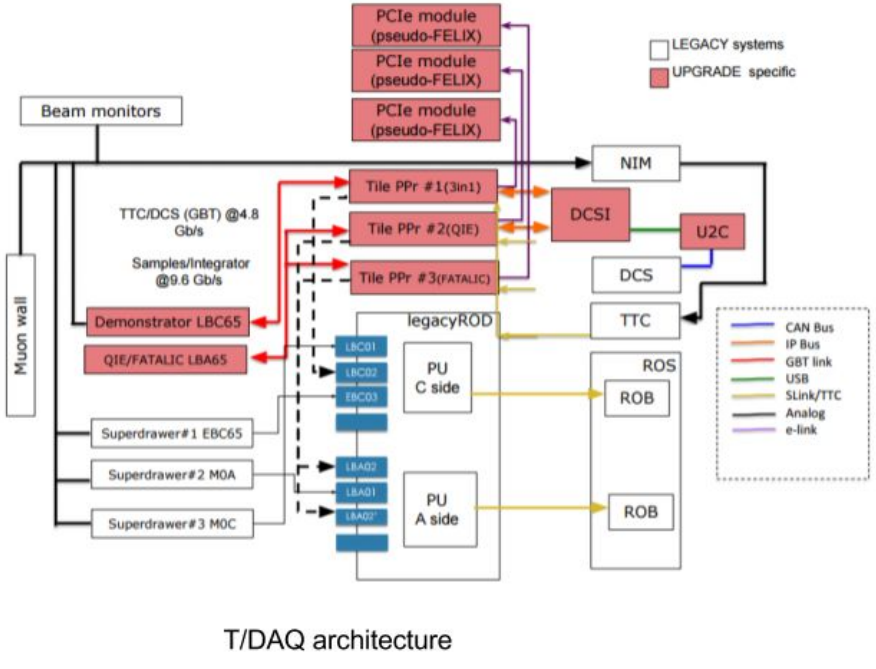
Drawer modules



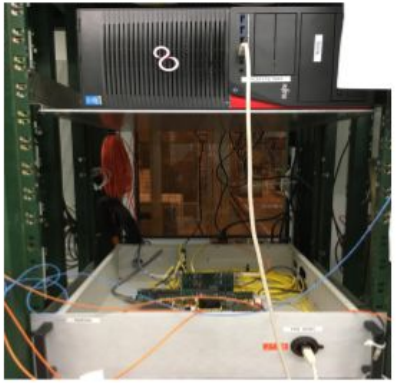
Back-end electronics

- Demonstrator (3-in-1, QIE and FATALIC) drawers have been inserted into TileCal modules.
- 3 other modules equipped with current systems electronics included for comparison.
- Using same DAQ software releases as running in ATLAS experiment.
- 3-in-1 option is readout using both the PPr and the Legacy BE electronics since it is the only option providing analog trigger signal (Backward compatibility).

T/DAQ CONFIGURATION @ TESTBEAM



T/DAQ architecture



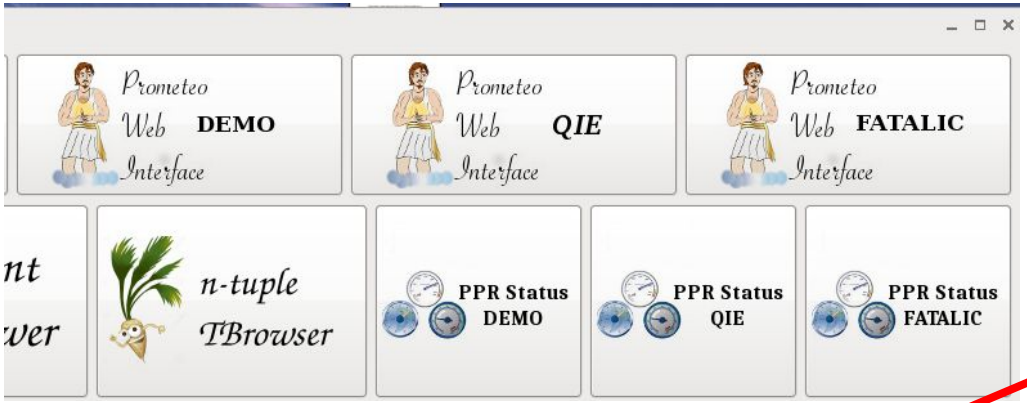
3-in-1 PPR → FELIX

QIE/FATALIC → FELIX

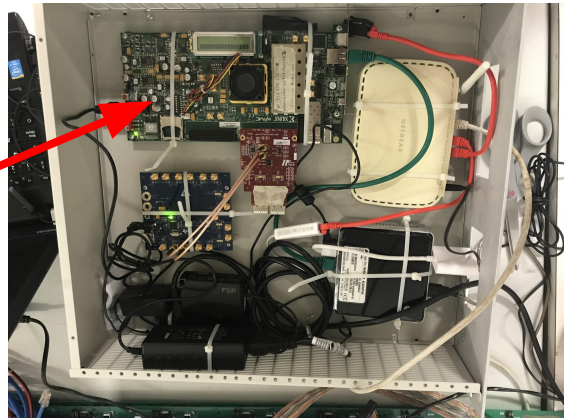
FELIX is a PC-based multi-interface device designed to mediate between ATLAS detectors which use the GBT protocol , and the ATLAS DAQ system.

T/DAQ PPr SOFTWARE

- Quick access status checks for PPR and Prometeo Interface.
- Communication via the IPBus hub.
- PPr monitoring - links configuration
- Expert Prometeo Web based Panel.
- Prometeo- a portable testbench for the FE electronics
- Up to 3 PCIe pseudo-FELIX operated in parallel with common PPr firmware and software.
- Prometeo components (HV, LED, ADC boards) and enclosure manufactured in South Africa.

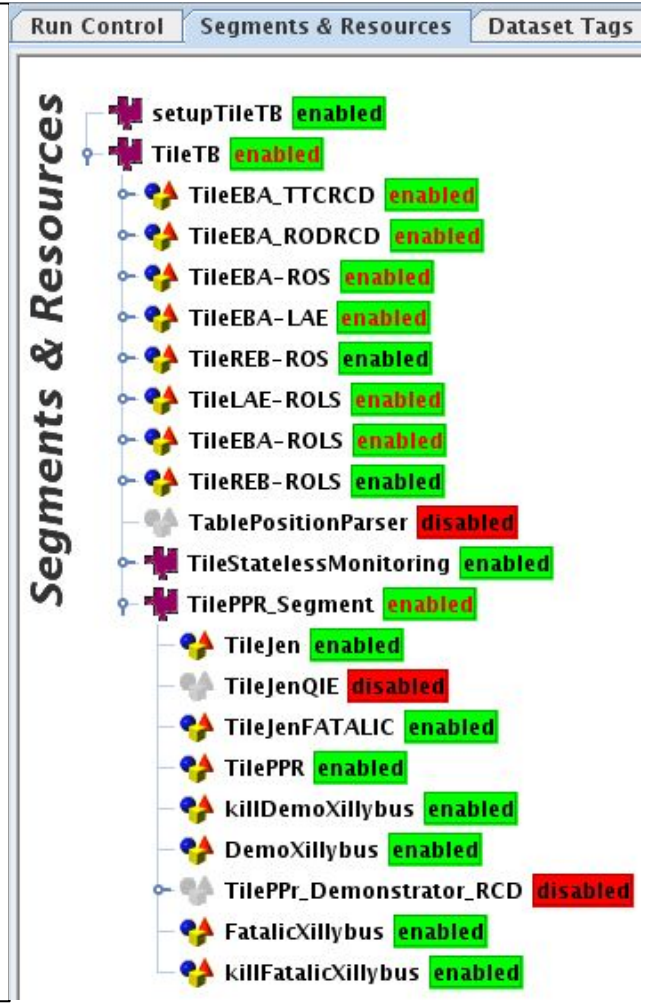


Prometeo - PPr Emulator

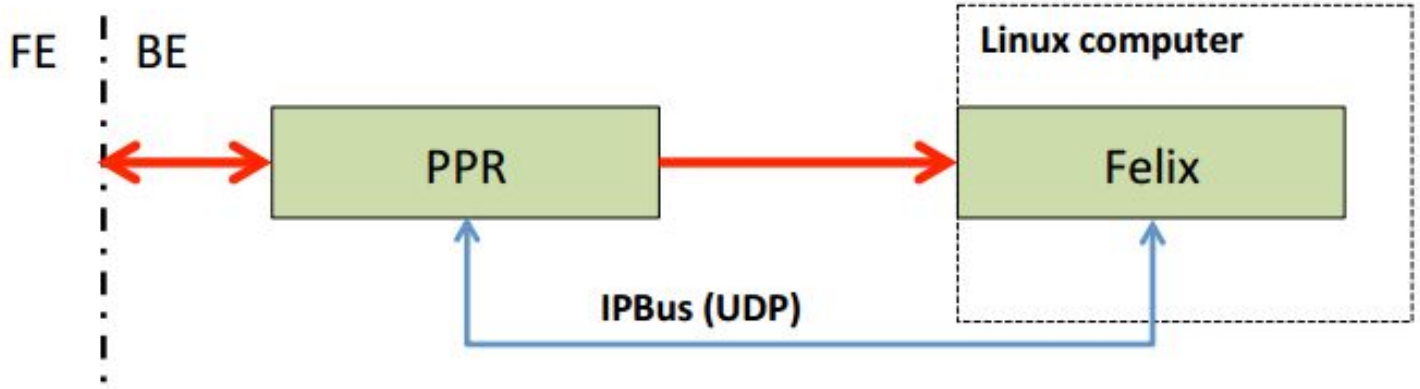


T/DAQ PPr SOFTWARE

- Demonstrator
  - Backward compatibility with TTC and TDAQ
  - Special segment in TDAQ for configuration
  - Calibrations in TDAQ infrastructure
  - DQMD (Data Quality Monitoring Display)
- TilePPR_Segment for PPr specific control and configuration.
- Readout through FELIX emulator with Xillybus ipcore.
- FELIX emulator readout
  - ASCII- saves formatted stream on local disk.
  - Binary- saves data in raw binary format, allowing ATLAS data format.
- Upon the reception of a L1 (trigger) Accept signal:
  - Pack the data with legacy data format and send events to old Readout Driver (ROD) through SFP.
  - Needed for backward compatibility with legacy DAQ for installation in P1 before Phase-II.
  - We need to accomodate the data to old data format (only 7 samples, 10 bits samples).
- Pack data with full precision and send it to FELIX.
  - Event: 16 samples x 16 bit x 12 channel x 2 gain = 6.2 kbit / mini drawer.
  - Max rate: Testbeam: 10 kHz → 62 Mbit/s → 8 bit elink / mini drawer
  - Max rate: P1 : 100 kHz → 620 Mbit/s/mini drawer



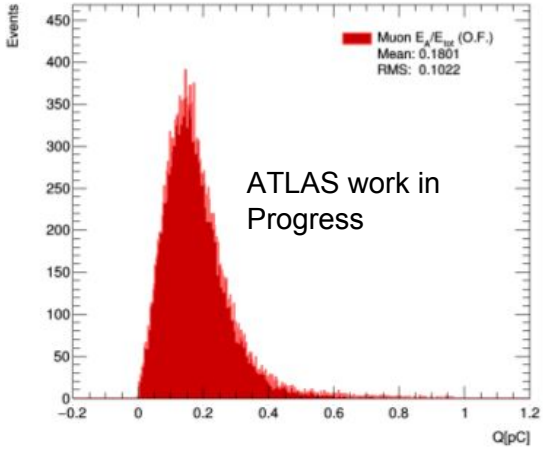
T/DAQ PPR TESTS WITH FELIX



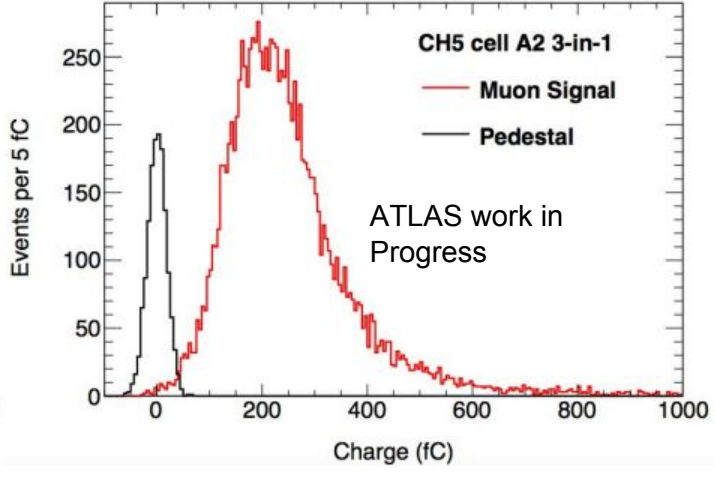
- Continue using the FELIX emulator for the testbeam in June and we will move to the official one for September.
- In TDAQ the PPr sends the data samples in parallel to the ROD (7 samples, 10 bits) and to FELIX (16 samples, 12 bits).
- Slow integrator (calibration and lumi measurement)
  - Continuos slow charge integration for each channel to FELIX.
  - 19 kbit/sec → 2bit elink /mini drawer.
- Finalize FELIX binary readout;
  - Need better mechanisms for data synchronization.
- Stream FELIX data to TDAQ for validation of ATLAS data format.
- Control through IPBus, useful for calibration runs.
- Monitoring available for the Legacy system and the Demonstrator through the ROD emulator.
- Start/stop controlled through python scripts, well tested with small issues.

TEST WITH BEAM SETUP RESULTS (MUONS)

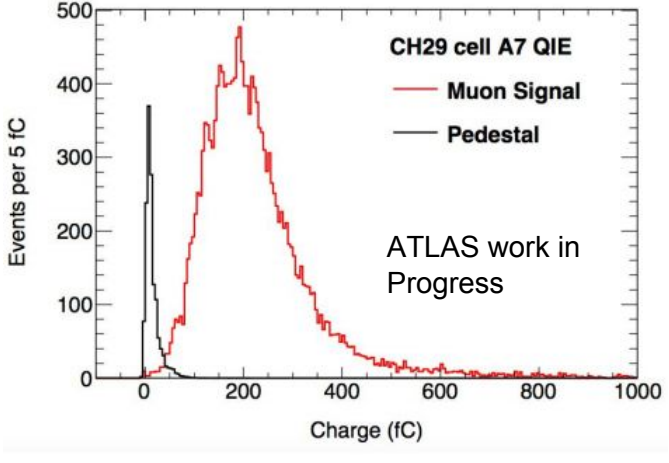
- The new 3-in-1, QIE and FATALIC systems were calibrated and evaluated with test beams muons in 2015, 2016 and 2017.
- The results speak of a strong upgrade system.
- Results from Muon Beam with energy of 200 GeV.
- Data is as simulated from EM scale (1.05 fC/GeV) and Monte-Carlo.



FATALIC



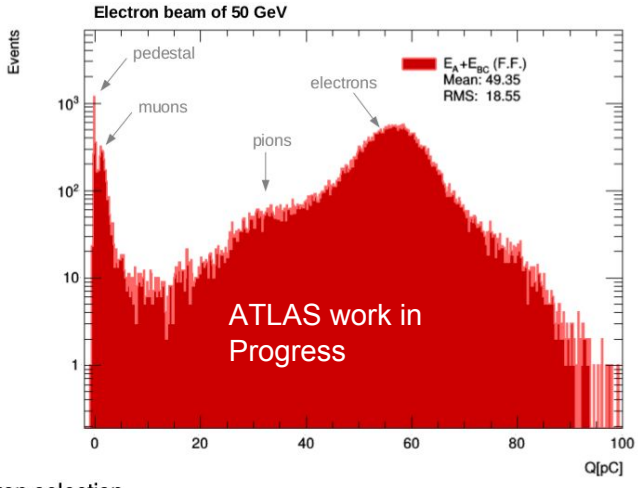
3-in-1



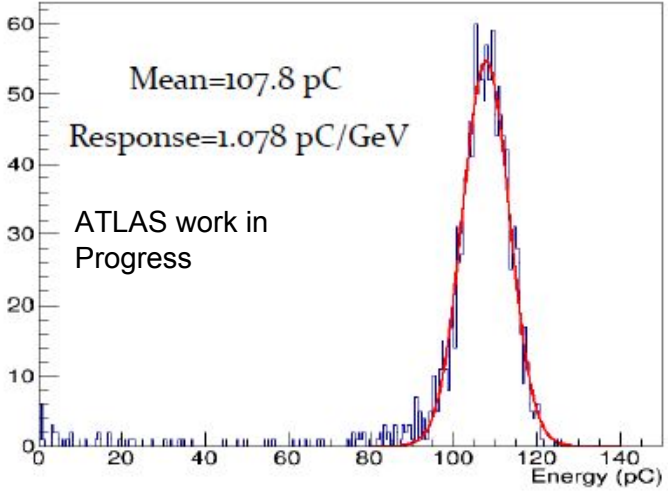
QIE

TEST WITH BEAM SETUP RESULTS (ELECTRONS)

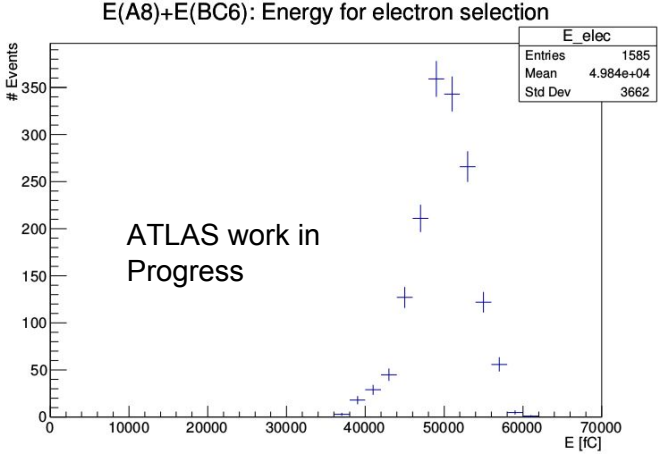
- The new 3-in-1, QIE and FATALIC systems were calibrated and evaluated with test beams electrons in 2015, 2016 and 2017.
- The results speak of a strong upgrade system
- Electron beam with energy of 50 GeV for QIE and FATALIC .
- Electron beam with energy of 100 GeV for 3-in-1.



FATALIC



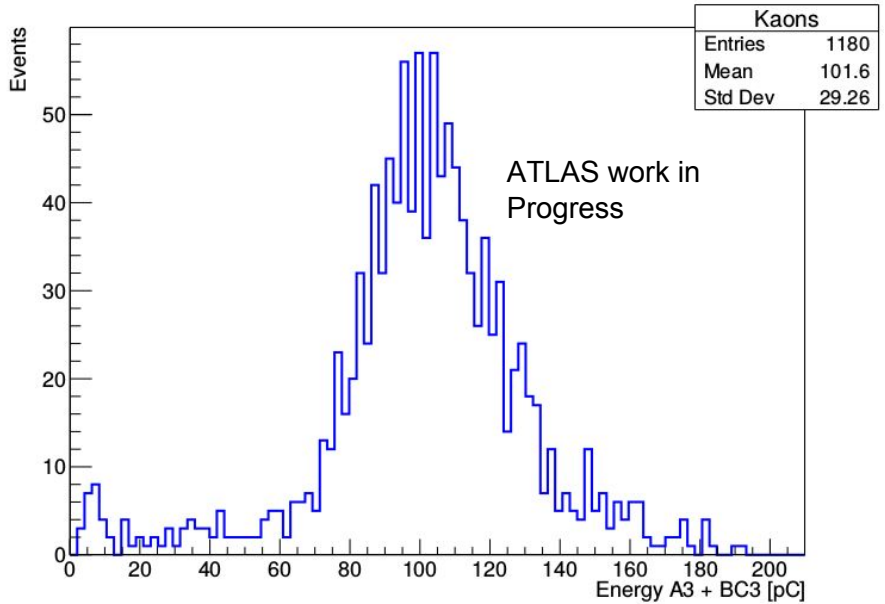
3-in-1

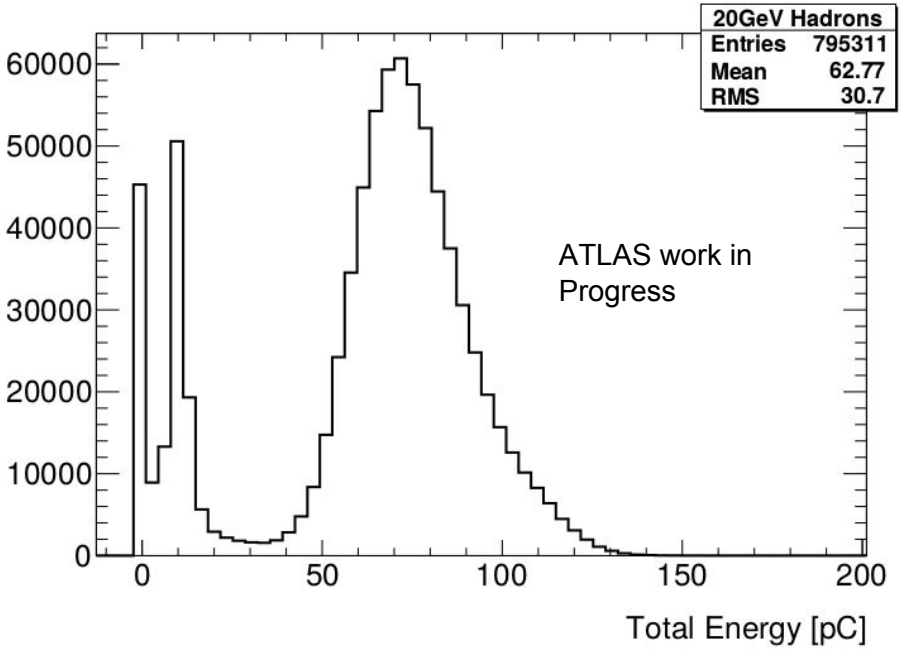


QIE

TEST WITH BEAM SETUP RESULTS (HADRONS)

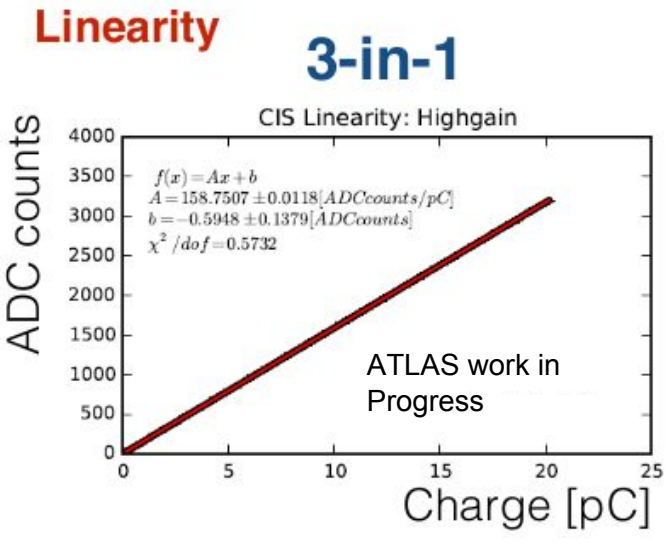
- The new 3-in-1, QIE and FATALIC systems were calibrated and evaluated with test beams hadrons in 2015, 2016 and 2017.
- The results speak of a strong upgrade system
- The EM scale was increased by 5x for hadron studies.
- This is only done for 3-in-1 Demonstrator and the results are shown for 20 GeV hadron beam.
- The total calorimeter energy is shown.

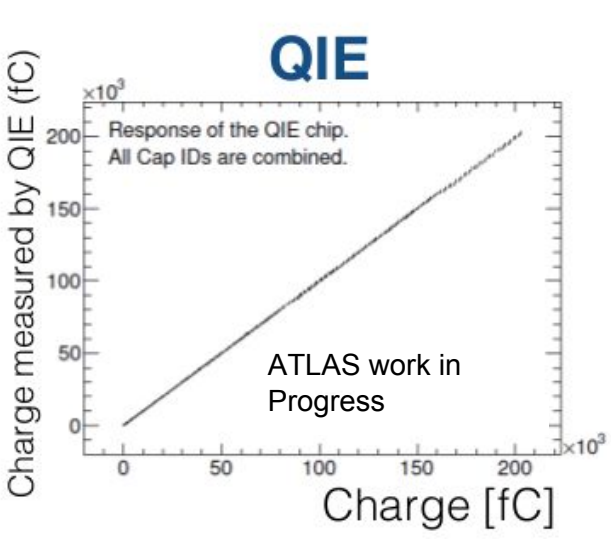


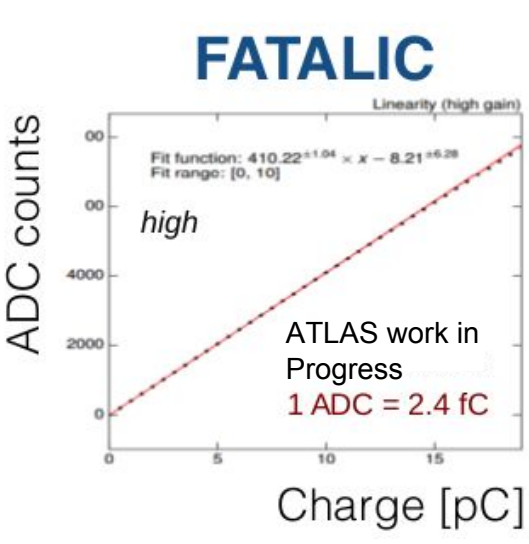


SYSTEM LINEARITY TESTS

- QIE - A well-known injected current is measured simultaneously with QIE and the current integrator.
- 3-in-1- A known charge charge is injected into the PMTs and measured through the 3-in-1 card.
- FATALIC - Similar to the 3-in-1, but signal is measured by the FATALIC chip.
- All systems working well within simulated specifications.







CONCLUSIONS

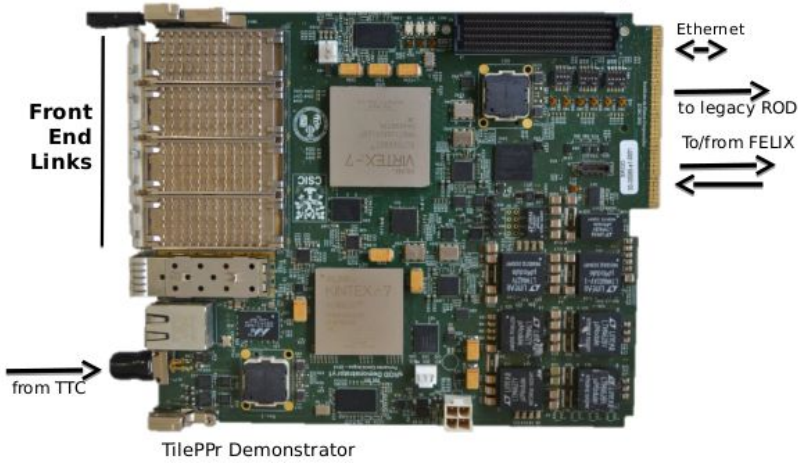
- TileCal Upgrade will happen in Phase-II (2023)
  - But we want to use the official FELIX during test beams and in P1 when Demonstrator is inserted (maximum 4 FELIX links).
- Preliminary tests showed that we can receive TTC signals (clock, L1A, BCRs) and we can send data packets to FELIX.
  - Save data and decode our data fragments within boundaries introduced by FELIX.
- Next steps:
  - Update the Gigabit Transceiver (GBT) firmware version.
  - Study the maximum trigger rate to save data on disk for 4 elinks.
  - Integrate the acquisition with the TDAQ software.
- Upgrade activities are progressing well with the goal of test-beams to do performance analysis for the 2017 option down-selection.
- The reliability and stability of the system has been visibly improved with respect to the 2015 TB.
- The upgrade architecture is mature and well understood.
  - “3-in-1” and QIE FE technologies were successfully evaluated with test beams and do not need any major revisions.
  - FATALIC_5 revision has been tested in 2017 and the results speak of a strong technology. The digital data path and detector control worked well.
- All the results from 2015/16 test beam campaigns are documented in the Initial Design Report (IDR).

Thank You!!

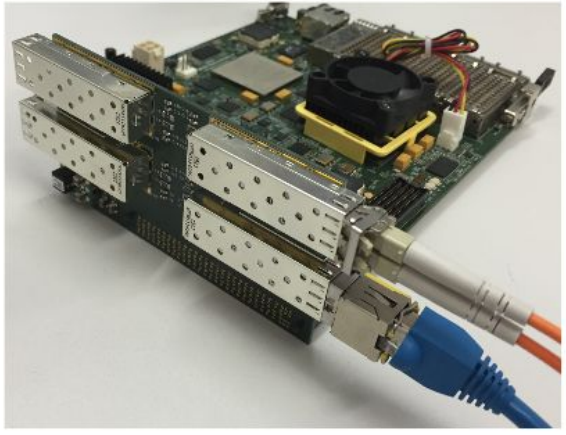
DEMONSTRATOR CHANGES WRT TO 2015

- New hardware components
  - DBv4: No CDCE but GBTx (GigaBit Transceiver) for clock recovery, Remote FPGA reset (more_on_GBT)
  - Mainboard v2: Frame/bit clock for ADC de-serialisation; Correct channel orientation + new 3in1 cards
  - PPr prototype: new module, no auxiliary boards, operation at 40.08 MHz (4,8 Gbps - 9,6 Gbps), firmware optimisations
    - Common PPr firmware for the 3 Front-End option.

- PCIe module for read-out (basic pseudo-Felix) - kc705 dev module - PCIe
  - GBT link/data-format compatibility with official FELIX
  - Free the IPbus for control, DCS and monitoring
  - Run parameters fragment (run number, L1ID, BCID, calibration)
- New DCS firmware (DB and PPr)
- Mobile Cesium unit in test-beam to perform in-situ Cs calibration runs (New in 2016)

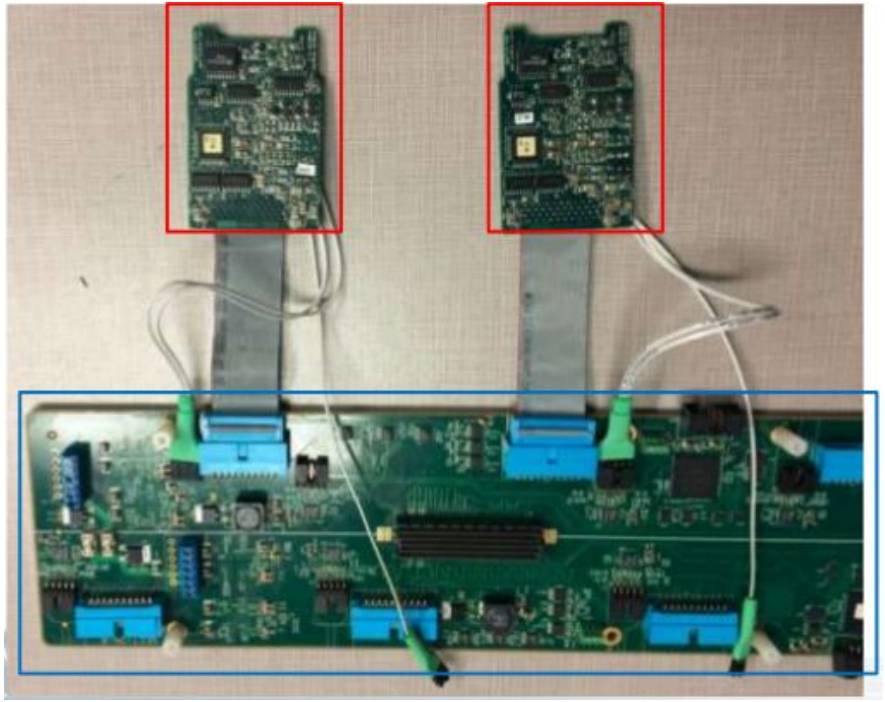


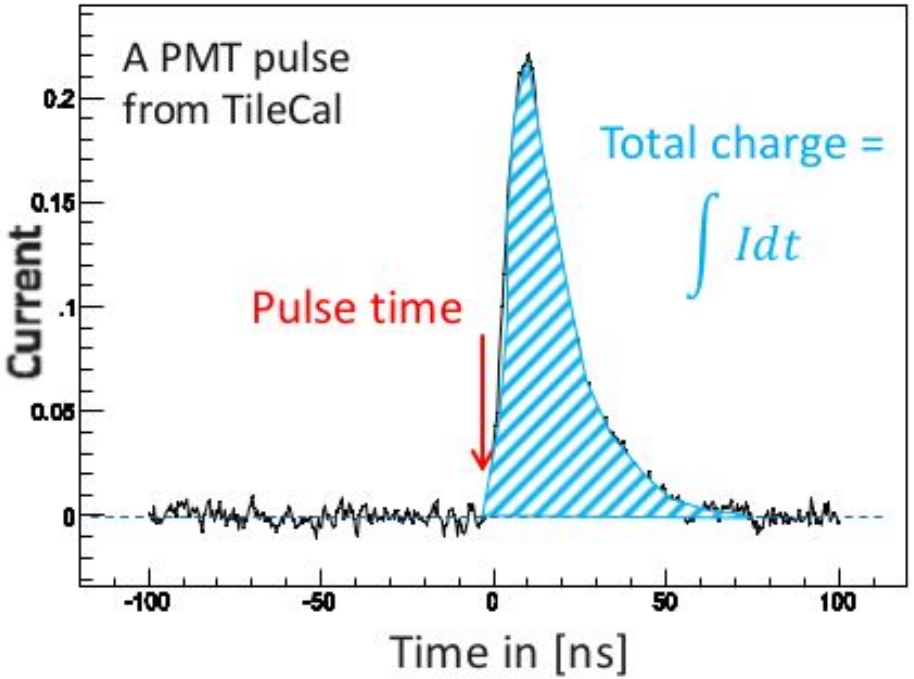
TilePPr Demonstrator



3-IN-1 SIGNAL PROCESSING

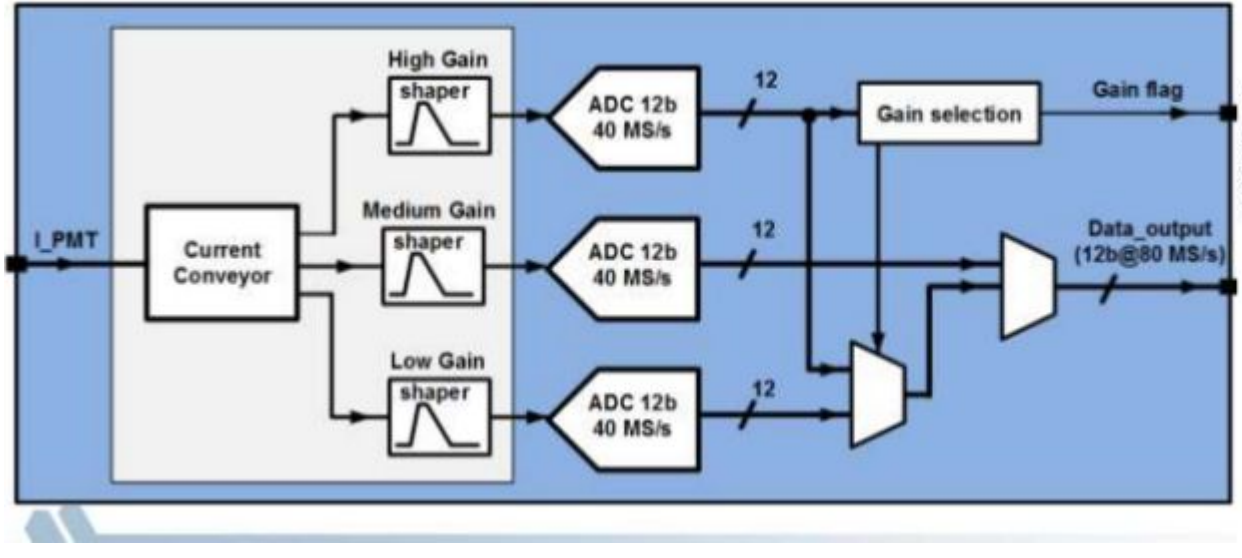
- The 3-in-1 signal processing approach uses a shaper circuit to transform a PMT pulse into an easy to digitize waveform/pulse whose amplitude is proportional to the total charge of the original PMT pulse.
- This approach is presently used in TileCal.
- The shaper circuit contains only passive elements and its performance is very predictable and well-characterized with calibration procedures.

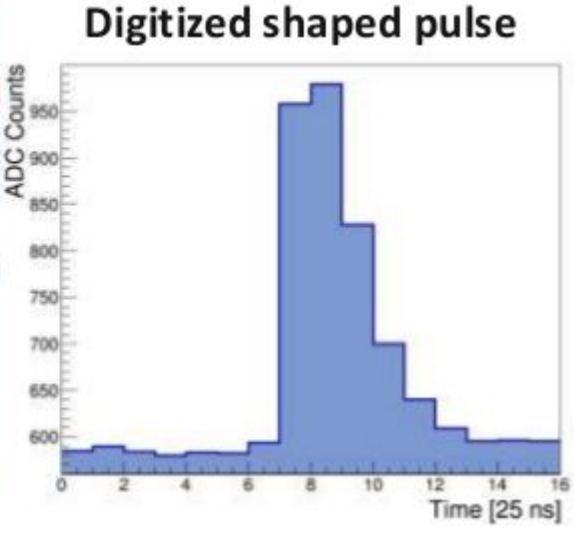




FATALIC SIGNAL PROCESSING

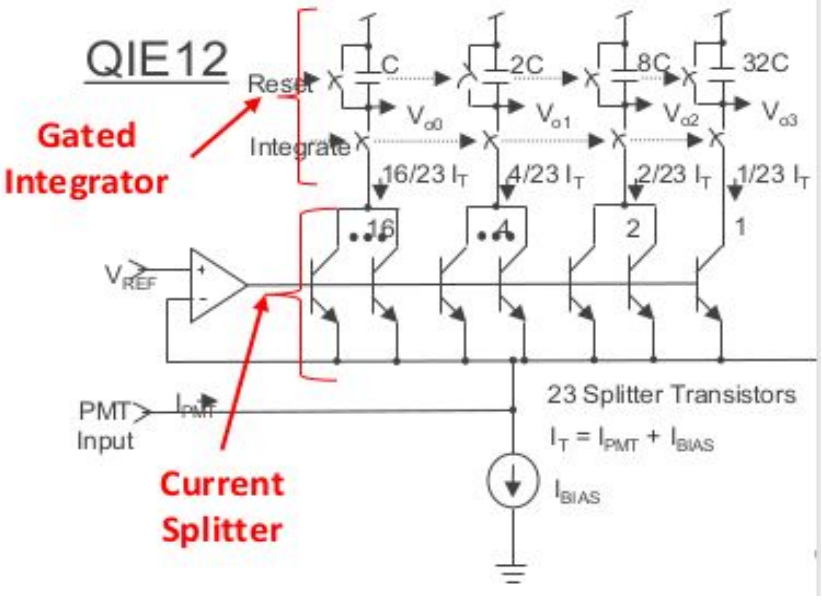
- The FATALIC approach also uses shaping like the 3-in-1 but the pulse shape is different.
- Digitization is done inside the chip.

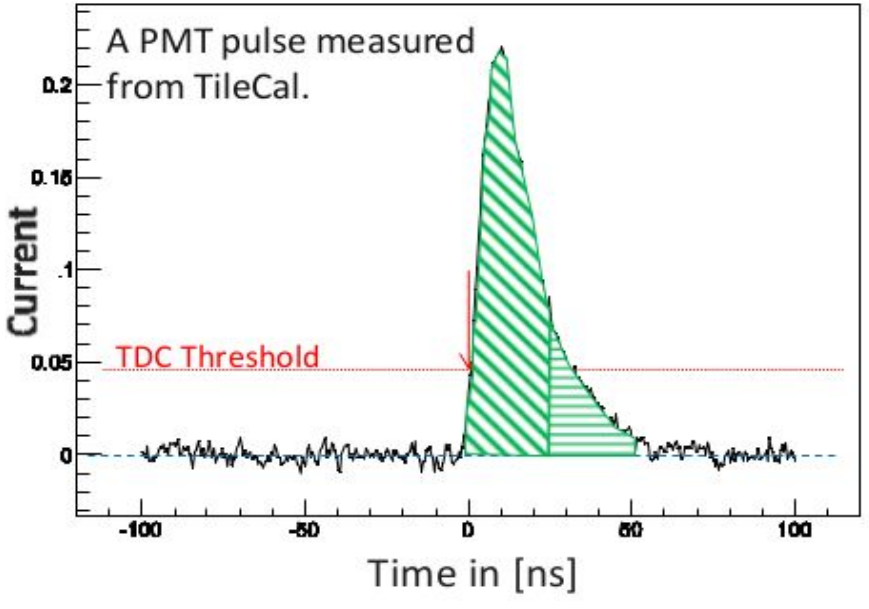




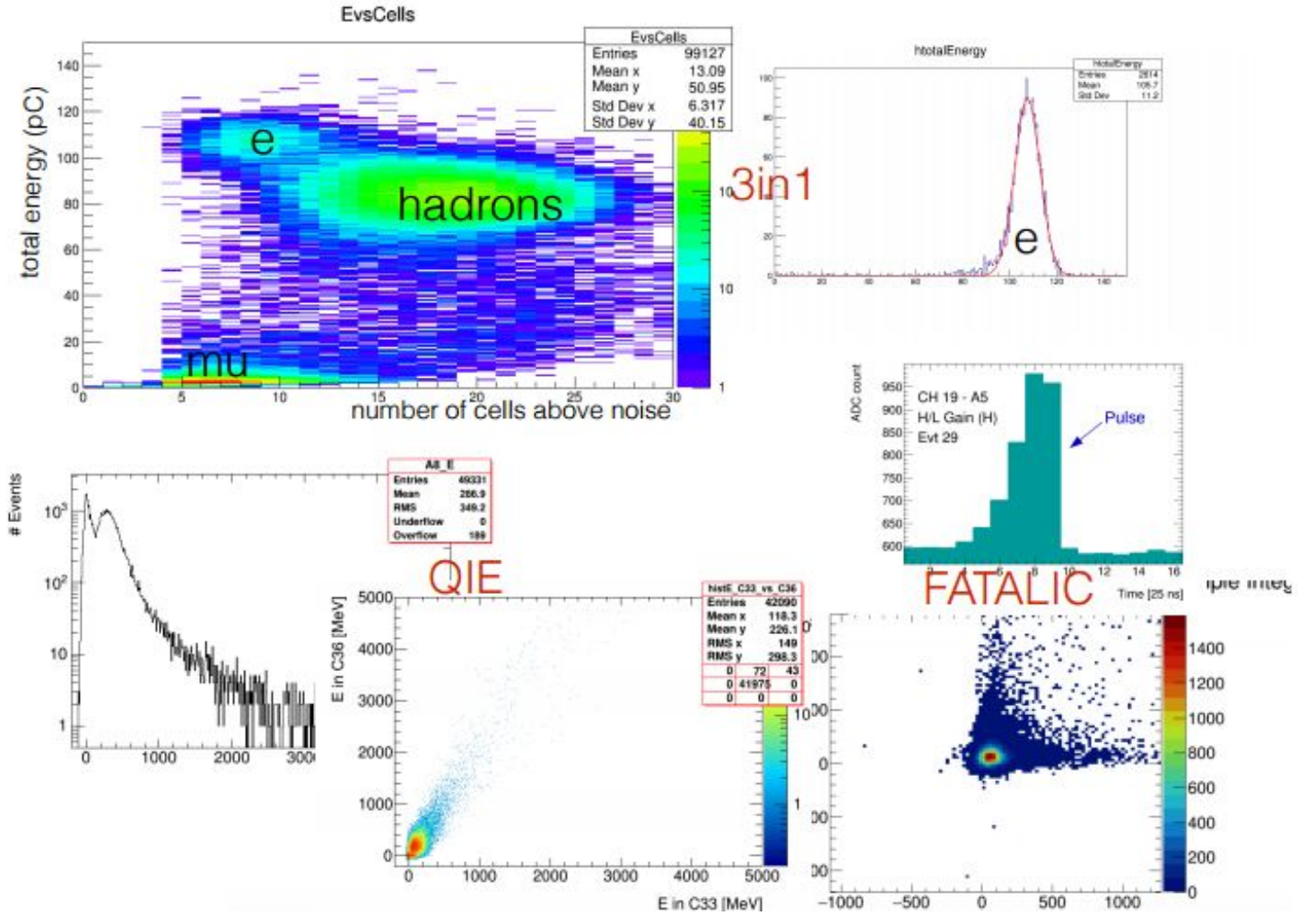
QIE SIGNAL PROCESSING

- The QIE circuit does not shape the PMT pulse to be digitized at 40 Msps.
- Instead, it directly integrates the PMT anode current in 25 ns intervals.
- Every 25 ns a QIE gives two numbers:
  - Charge (current integrated over a 25 ns period).
  - Time (when current crossed a threshold). 1 ns resolution
- The total charge of a PMT pulse (energy) is obtained as a sum of two or three QIE samples

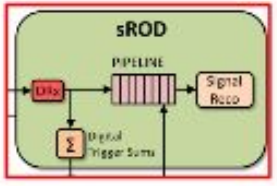




ANALYSIS FROM DIFFERENT FEB



PPr PROTOTYPE



TOP
BOTTOM

MiniPOD TX
- 12 x 10 Gbps
- L1 trigger communication

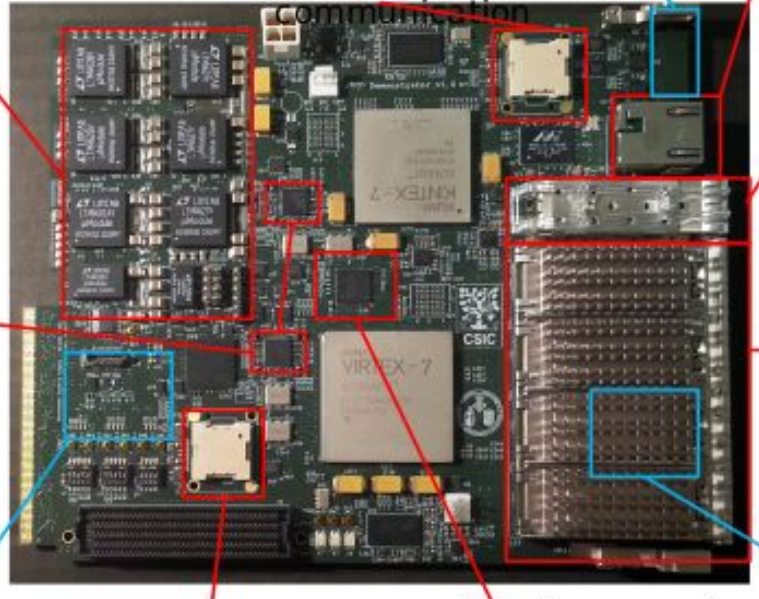
UART-USB ports

Ethernet port
- 10/100/1000 Mpbs
- PC communication

Power Modules
- Linear Technologies
- Low noise

Jitter cleaners
- TI CDCE62005
- Low jitter (< 1ps)
- Clean recovery clocks for GTX
- Unify clock domains

Power supervisory IC
- LT LTC2977
- Power sequencing
- Protection
- Current, voltage, temp.



SFP module
- TTC reception
- Communication with current DAQ system

4 x QSFP modules
- FE communication
- Each module at 40 Gbps
- Total max. BW: 160 Gbps

JTAG programmer

MiniPOD RX
- 12 x 10 Gbps
- Test purposes

Clock generator
- LMK03806B
- 10 diff outputs
- Low jitter

READOUT PRINCIPLE STRATEGY