Trigger and data acquisition systems readout architecture of the Tile PreProcessor Demonstrator for the ATLAS Tile Calorimeter phase-II upgrades

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Abstract. The LHC has planned upgrades culminating in the High Luminosity LHC which will increase of order at least 5 times the LHC nominal instantaneous luminosity in order to increase the potential for discoveries. This major increase in luminosity presents significant challenges in the form of increased trigger rates and detector occupancy. The ATLAS trigger and data acquisition systems will be upgraded in order to cope with the increased luminosity foreseen with the LHC upgrades. The ATLAS Tile Calorimeter will be upgraded as well following the ATLAS detector developments. The readout electronics for the Tile Calorimeter will be redesigned, adopting a new readout architecture. A Demonstrator program has been initiated to evaluate and qualify the readout architecture before full installation in phase-II. In the Demonstrator, the on-detector electronics will transmit readout data for every bunch crossing to the off-detector Tile PreProcessor. This Tile PreProcessor stores the data in pipeline buffers and upon reception of an external trigger signal the event data is processed, packed and readout through the legacy system, the new ATLAS proposed FELIX system and an ethernet connection for monitoring all in parallel. A series of test with beam setup campaigns took place between 2015 and 2017 to evaluate the phase-II upgrade electronic prototypes in the lab and to help with estimate provisions for future commissioning efforts. The primary objective of this campaigns is to assess the status of the Demonstrator based on the modified 3-in-1 front-end board baseline option and to give some attention to QIE and the FATALIC. This contribution describes the various aspects of the proposed phase-II readout architecture..

1. Introduction

The hadronic Tile Calorimeter (TileCal) is the central region of the ATLAS experiment at the Large Hadron Collier (LHC) and is used for the energy and direction measurements of hadrons, jets and leptons. It is a large sampling calorimeter which makes use of steel as the absorber material and plastic scintillating plates readout by 9852 Photomultiplier Tubes (PMTs) through wavelength shifting (WLS) fibers [1]. The signals and data from the detector are processed by the Trigger and Data Acquisition (TDAQ) system. The trigger selects event fragments with distinguishing characteristics in real time. The DAQ receives event fragments, reads them out through the Readout System (ROS) and feeds them to the software based high level trigger. The DAQ also provides control, configuration and monitoring functionalities [2]. The High Luminosity LHC (HL-LHC) is a proposed upgrade project termed phase-II and is aimed at cranking up the performance of the LHC by increasing the luminosity to an order at least 5 times beyond the nominal value in order to increase the potential for discoveries after 2025 [3].

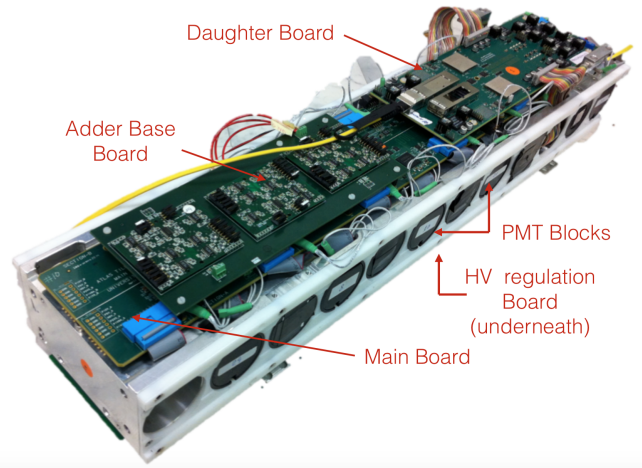


Figure 1: A rendering of a Tile Calorimeter mini-drawer and the components it comprises.

The large luminosity of course offers the opportunity for a wealth of physics measurements, but presents significant challenges to the detector and the TDAQ systems in the form of increased trigger rates and detector occupancy. This mandates an upgrade of the entire ATLAS TDAQ system in order to cope with the HL-LHC. TileCal plans to undergo upgrades as well following the ATLAS detector developments imposed by the HL-LHC. It is currently envisaged that the detector components (iron absorbers, scintillating tiles and optical fibers) will not be changed because they are still in good shape. The current readout architecture outputs digital data at a maximum rate of 100 kHz with a maximum latency of up to 3 μs and stores it in 6 μs pipelines , it is basically not compatible with the baseline trigger architecture of the HL-LHC. The detector readout electronics will be completely replaced to accommodate the new two-step Level-0/1 architecture: the higher trigger accept rates and the extended latencies at both Level-0 (L0) and Level-1 (L1). A new TDAQ architecture is to be adopted to provide full digital calorimeter granularity at the first level of trigger. The digitized data from every bunch crossing will be readout by the off-detector PreProcessors (PPr) [4]. In order to qualify the new proposed readout architecture and the first prototypes of the different components, TileCal has undertaken a series of tests with beam setup campaigns at the CERN accelerator facilities. TileCal prototype drawer modules termed Demonstrators have been instrumented with upgrade specific electronics together with other modules instrumented with current legacy system electronics were exposed to different particles (hadrons, electrons and muons) at different energies during 4 campaigns between 2015 and 2017.

2. TileCal Phase-II electronics Upgrade

For phase-II, the front-end (FE) electronics will be housed in independent mechanical structures called mini-drawers (see Fig. 1). Four mini-drawers comprise a super-drawer in contrast to the current configuration of 2 drawers. This particular stacking was done to improve reliability of the interconnections and to avoid single-point failures due to power distribution in particular. Each mini-drawer houses a total of 12 PMTs with FE amplifier cards for pulse conditioning and calibration, a main board (MB) that receives PMT signals and routes them to the Daughter Board (DB) which handles all communication with the back-end (BE) electronics, an adder base board which is only needed for analog trigger signals aggregation in the 3-in-1 Demonstrator, and lastly, a High Voltage (HV) regulation board to deliver the correct HV to the PMTs [5].

The proposed TileCal TDAQ architecture for phase-II is shown in Fig. 2. The readout is based on a continuous digitization and data transfer to the off-detector Tile PPr for very bunch

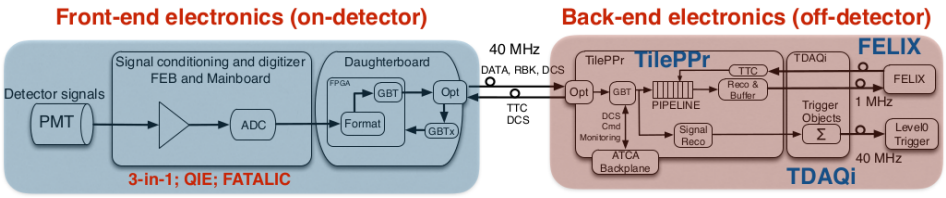
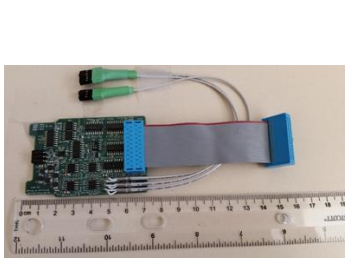
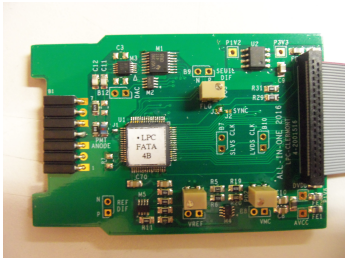


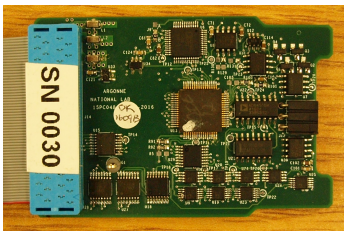
Figure 2: The TileCal phase-II upgrade readout architecture.



(a) 3-in-1 FEB.



(b) FATALIC FEB.



(c) QIE FEB.

Figure 3: The 3 Tile front-end cards under evaluation for phase-II.

crossing (40 MHz) of all readout channels. The design has fair emphasis on redundant optical transmission of the data, this means that no gain selection logic will be implemented in the FE electronics and the digitized signals of both gains will be transmitted. Pipelines and the de-randomizer are implemented by the PPr units located in a low radiation environment of USA-15. The PPr will further apply energy scale calibrations as in the current Readout Drivers (ROD) and prepare the L0/1 trigger information [6].

3. Changes and options

3.1. Front-End

TileCal R&D program includes three different front-end board (FEB) options for processing PMT signals as shown in Fig. 3. One of the options under consideration is an optimized redesign of the current 3-in-1 FEB that uses state-of-the-art discrete commercially off-the-shelf integrated circuits. The 3-in-1 signal processing approach uses a shaper circuit to transform a PMT pulse into an easy to digitize waveform/pulse whose amplitude is proportional to the total charge of the original PMT pulse. The shaped signal is then amplified in two separate ranges and sent to 12-bit ADCs on the MB [4].

Another approach is the Front-End ATLAS Tile Integrated Circuit (FATALIC) which uses shaping just like the 3-in-1 but with a different pulse. This ASIC chip is a new technology for TileCal and aims at integrating much of the 3-in-1 functionality into the FATALIC chip, this includes signal digitization. The ASIC design is based on a 130 nm CMOS process which has been already qualified in ATLAS for applications in other subsystems with much higher radiation doses [7].

The third option is the Charge Integrator and Encoder (QIE) ASIC developed by Argonne National Lab. The QIE circuit does not shape the PMT pulse to digitize at 40 MHz. Instead, it directly integrates the PMT anode current in 25 ns intervals. This chip has been designed to satisfy the radiation requirements tailored for TileCal. QIE offers a unique opportunity to reduce the impact of the out-of-time pileup measurements for TileCal [8].

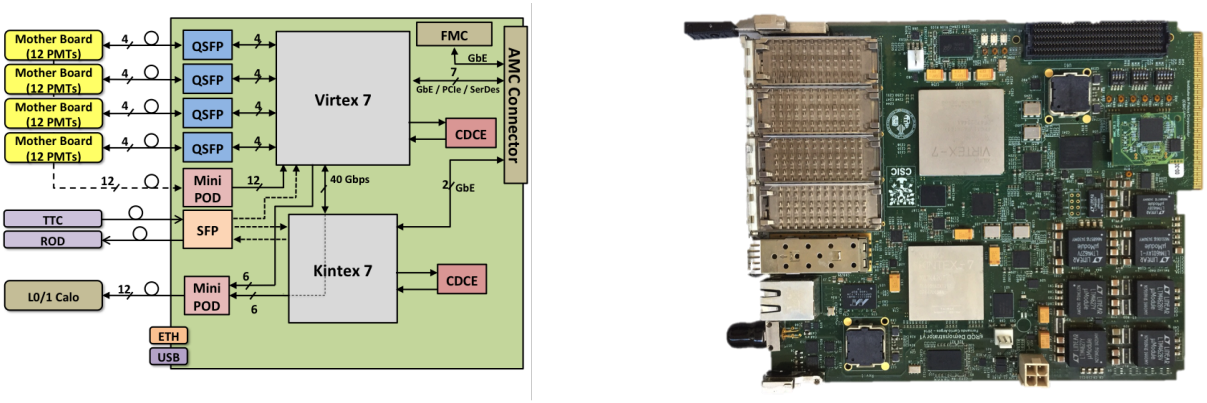


Figure 4: A sketch representation of the Tile PPr board (left), and the PPr AMC board (right).

3.2. Back-End, PPr

Figure 4 shows a sketch of the Tile PPr. The PPr is the core of the BE electronics system and provides benchmarks for investigating the different parts of the upgrade system. It is a high performance double advanced mezzanine board based on FPGA (Field Programmable Gate Array) resources and QSFP (Quad Small Form-Factor Pluggable) modules. This board has been designed in the framework of the ATLAS TileCal Demonstrator project for the phase-II upgrades as the first stage for the BE electronics. The data is received through four optical connectors and the internal hardware transceivers located in the main FPGA. This FPGA also contains the pipeline and de-randomizer memories, the synchronization of data with TTC (Timing, Trigger and Control) and the reconstruction of the events passing the L0/1 trigger. The L1 calorimeter (L1Calo) preprocessor module implements the algorithms to provide digital information to the L0/1 trigger of ATLAS. The new architecture of the read-out improves the precision and the granularity of the trigger information for the cluster and jet energy L1Calo processors. The increased granularity can be achieved in the radial direction, which would eventually allow the implementation of shower profile algorithms at L0/L1. The use of digital signals at the PPr for the L0/L1 trigger replaces the present analog L1 trigger preprocessors. The board transmits the data accepted by the L0/L1 trigger to the ROS. In addition, the board is the BE interface with the DCS (Detector Control System) and TTC of the FE electronics [9].

3.3. Demonstrator project

The Demonstrator project aims at testing the long term performance of the upgrade system without compromising the present data taking. This is to be achieved by developing an early version of the new digital calorimeter system that is compatible with the present analog trigger, DAQ, DCS and TTC. Digital transformation will translate TTC signals into upgrade specific commands and translate upgrade outputs to a format acceptable by the present RODs. The TileCal Demonstrator is a prototype phase-II super-drawer composed of 4 independent mini-drawers (see Fig. 1). If verified to perform according to requirements a Demonstrator drawer is to be inserted into the real ATLAS detector. If this is successful, three more additional Demonstrator modules will follow in one of the short end of year Christmas shutdowns [10]. This will allow thorough testing of the major functionality of a phase-II system before full installation in phase-II. The data is readout readout through the PPr board which formats and transmits to the legacy RODs for backward compatibility with current system and to the Front-End Link eXchange (FELIX) [11] as presented by Fig. 5.

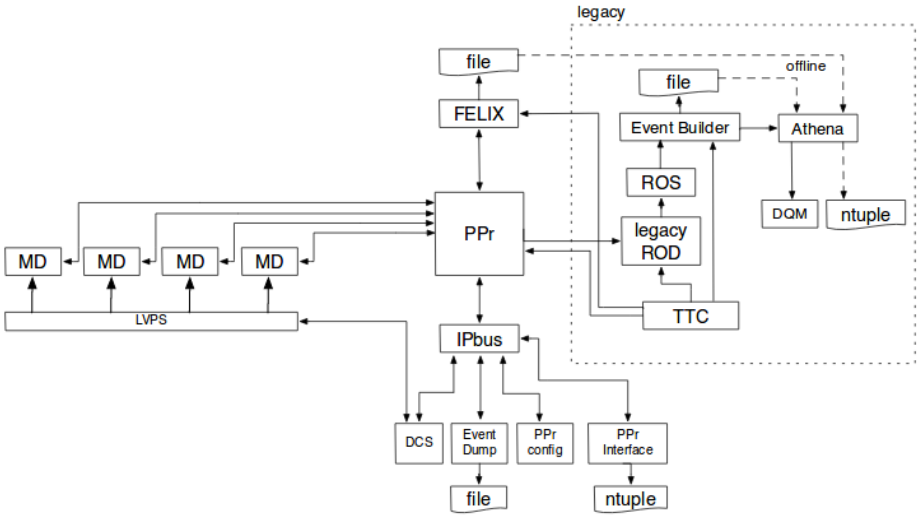


Figure 5: Demonstrator data acquisition architecture with PPr.

4. Test Beam campaigns

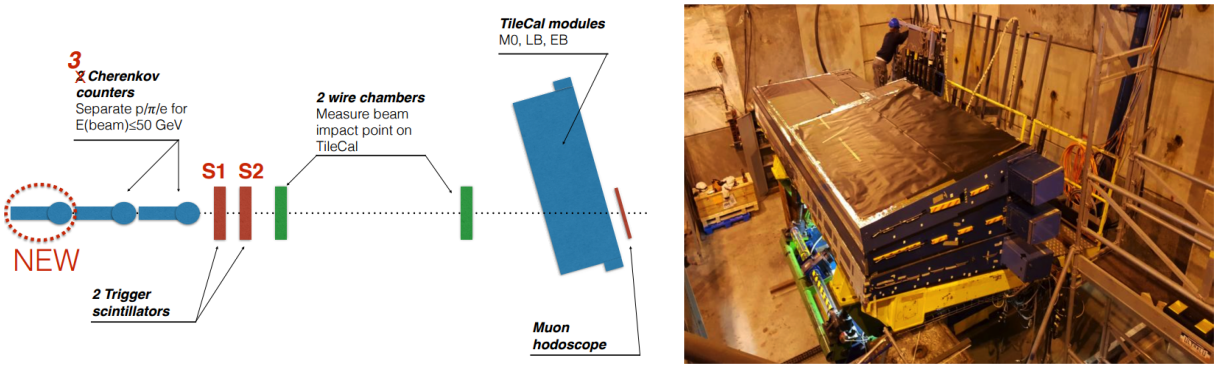


Figure 6: Diagram of the beam elements (left), and a picture of the TileCal modules mounted on a mobile table.

A series of test with beam setup campaigns took place between 2015 and 2017 to evaluate the phase-II upgrade electronic prototypes and to help with estimate provisions for future commissioning efforts. The primary objective is to assess the status of the Demonstrator based on the modified 3-in-1 FEB baseline option and to give some attention to QIE and FATALIC. A hybrid Demonstrator that uses the 3-in-1 option has been developed and is fully compatible with the current system providing both the analog trigger signals for the current L1 trigger and full digital information for the phase-II PPr prototypes. In parallel, one more TileCal module has been instrumented with the two other options, and three other modules equipped with current legacy system electronics were exposed to muons, electrons and hadrons at different energies during this test beam campaigns to assess their performance. The results from these campaigns provide the necessary performance analysis to aid the 2017 FEB option down-selection. Some preliminary results from the 2016 test beam campaigns are accessible here [5,12]. Figure 6 shows the module configuration for the tests with beam setup campaigns at the CERN beam facilities.

The prototype PPr was used during this campaigns since it can be operated in both legacy and upgrade modes as shown by Fig. 5. In legacy mode, the PPr emulates the legacy FE

electronics by receiving data samples at 40 MHz and stores it in pipeline memories and packs with the legacy L1A signals to be transmitted to the RODs through optical links. The ROD performs further processing and transmits to the ROS, and finally to the Event Builder which saves the data on disk. Synchronization of the Demonstrator data with the legacy system data is achieved using the clock and trigger information distributed by the legacy TTC modules. The PPr implements a trigger identification algorithm to the data packets and synchronizes the two systems. In upgrade mode, the PPr transfers the L1A data through dedicated high speed optical links to the FELIX system which then saves the data on local disk for offline reconstruction and analysis. There is a PPr specific package called the PPrInterface used for standalone system verification tests. The 3-in-1 Demonstrator was readout using both upgrade and legacy readouts, whilst the QIE and FATALIC are only readout using the upgrade specific FELIX readout [5,10].

5. Conclusions

The High Luminosity LHC project will increase the luminosity by an order at least 5 times beyond the Run 2 nominal luminosity (L = 5 x 10^{34} $cm^{-2}s^{-1}$) in order to reach the design center of mass energy ($\sqrt{s} = 14$ TeV). The ATLAS trigger and data acquisition architecture will undergo upgrades to cope with the High Luminosity LHC, TileCal will also undergo upgrades following ATLAS developments. TileCal Demonstrator modules have been instrumented with initial phase-II upgrade electronic prototypes and assessed with beam setup at the CERN beam facilities during 2015, 2016 and 2017. Preliminary results speak of a strong, efficient and mature upgrade system. The operation of the Demonstrators and data analysis have been used to gain experience and identify weak points in the system. The tests with beam will continue to test the maturity of the Demonstrator for insertion into the real ATLAS detector and to improve understanding of the physics performance of the current system. This will be followed by the production and installation of the new system during the LHC Long Shutdown scheduled for 2025-2026.

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