The ATLAS Tile Calorimeter hybrid demonstrator

Matthew Spoor and Bruce Mellado Garcia

School of Physics, University of the Witwatersrand, Johannesburg, South Africa

E-mail: matthew.spoor@cern.ch, Bruce.Mellado.Garcia@cern.ch

Abstract. The LHC is currently preparing for the Phase II upgrade that is scheduled for 2022. Once upgraded the LHC will begin its high its High Luminosity Phase (HL-LHC) increasing the luminosity by a factor 5-7. This will vastly increase the amount of particles it could detect potentially addressing the unsolved mysteries such as dark matter. A new hybrid demonstrator prototype for the ATLAS TileCal is to be installed during the LS1. The demonstrator system needs to be fully compatible with current detector electronics as well as act as a validation for the new read-out architecture. This report gives overview of the on-detector and off-detector electronics used for the current demonstrator proposed for the Phase II.

1. Introduction

The Phase II upgrade [1] of the ATLAS detector will increase the original design luminosity by a factor of 5 to 7. There are number of upgrades that are planned for the ATLAS detector, with high radiation levels and increased data processing requirements there is a need for a complete redesign and replacement of the read-out electronics. Since the initial design there has been huge advances in technology leading to more advanced chips with greater radiation tolerances.

The current read-out system stores digitised samples in front-end electronics pipeline memories. Only samples that are selected by the L1 trigger are sent to the back-end electronics for further processing. The new electronics system will provide full digital readout of all channels that will be transmitted to the off-detector pipeline memories each bunch crossing (40 MHz) using multi-gigabit optical links. An improved back-end electronics system will now have to supply digital information to the First Level trigger per bunch crossing. This will provide digitally calibrated information with enhanced precision and granularity to the First Level trigger in order to improve both trigger latency and resolution. The new front-end architecture merges some boards to create a more compact 3 board system. Additionally new levels of reliability and redundancy have been introduced with many components being duplicated.

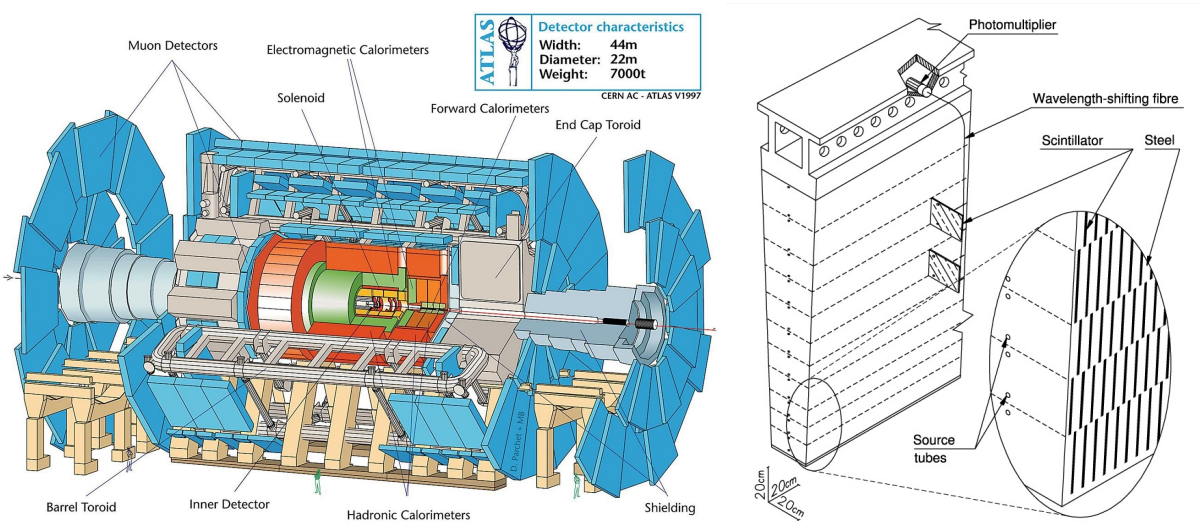
2. ATLAS Tile Calorimeter

The ATLAS (A Toroidal LHC AparatuS) experiment (Figure 1a) at the Large Hadron Collider (LHC) is a general purpose detector located at CERN. ATLAS comprises of several different sub-detector systems. The experiment was designed to record proton-proton collisions that occur every 50ns resulting in data flows in the 100s of GB per second range.

The Tile Calorimeter (TileCal) [2] is the central hadronic calorimeter of the ATLAS experiment. The TileCal is made up of 4 sections: two central barrels in the middle and two extended barrels on either side. Each of the four sections is divided into 64 azimuthal slices (Figure 1b). Within each slice there is a fine lattice of steel plates with plastic scintillating

tiles placed in-between. In total there are 430 000 tiles contained inside the TileCal making up 5000 calorimeter cells. Signals are recorded by 10 000 photomultiplier tubes (PMTs) linked to readout electronics. The Font-end electronics are stored within drawers at the back of every slice.

When particles enter the TileCal system they collide with steel plates which causes them break up into showers of charged and neutral particles. The TileCal has the critical role of measuring the energy and direction of these showers. As particles pass through scintillating materials they deposit tiny amounts of energy. Due to the molecular structure of tiles, this energy is converted into photons. Theses photons travel through the scintillators into wave length shifting optical fibers. This light is carried along the fibers to PMT modules where the light is converted into an analog electrical signal. The signal is then passed to the front-end electronics for amplification, digitisation and trigger selection after which they are sent to the back-end electronics for data formatting and further L2 trigger selection.



(a) (b)

Figure 1: a) Tile Calorimeter Detector b) TileCal module.

3. Present read-out electronics

The present font-end electronics is made up of four board types: 3-in-1 one Front-End board (FEB), 3-in-1 Mainboard (MB), digitiser board and Interface board [3]. The multipurpose 3-in-1 FEBs amplifies and shapes PMT signals into 27 ns pulses as well as provides calibration functions. The main board is responsible for the control and calibration of the 3-in-1 cards. The digitiser samples the analog pulses using both high and lows gains and stores them in pipeline memories. Low gain signals are merged in the adder board before being sent to trigger tower to be used for the L1 trigger. Data temporarily waits for trigger validation in the pipeline memory. If data is seen to be interesting it will be accepted by the trigger and sent to the Interface board where it is placed in derandomising buffers and read out. The Interface board will transfer data at 100 KHz to the Read out driver (ROD) to be formatted before being sent to the data acquisition system (DAQ) [2]. Data that is not accepted by the trigger will be written over once new data comes in.

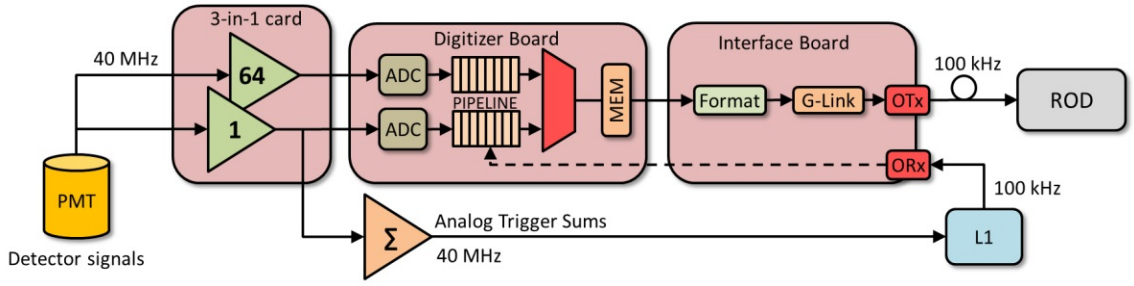


Figure 2: Present Tile Calorimeter readout architecture.

The current housing for the front-end electronics is made up of two 2m in length drawers forming a retractable superdrawer [4]. Each superdrawer can accommodate 4 MBs, 48 FEBs, 48 PMTs, 4 digitiser boards and one Interface board. The MBs of each draw are daisy chained together so all signals and power supplies are shared. This design has a single output to the Interface board for the entire draw.

4. Hybrid demonstrator

During the LS1 a new demonstrator prototype will be installed into an external slice TileCal for testing in Building 175 at CERN. The TileCal Demonstrator is essential for the validation of the performance of the new readout architecture, trigger system interfaces and the implementation of novel trigger algorithms before the complete replacement of electronics in Phase II upgrade [5].

A new front-end electronics architecture was proposed that divides each TileCal module into 4 separate minidrawers that are independent in terms of power, readout and configuration. Each minidrawer is water cooled and houses a Mainboard, daughterboard, 12 PMT modules and a High Voltage card. Four minidrawers can be mechanically connected to form a Superdrawer. The whole module communicates digitised data from each PMT channel through Quad 10 Gbps optical fibers every bunch crossing (40 MHz) to the sROD (Back-end). The downlink (sROD to Front-end) consists of four 4.8 Gbps links mainly used for FEB and HV configuration and DCS information.

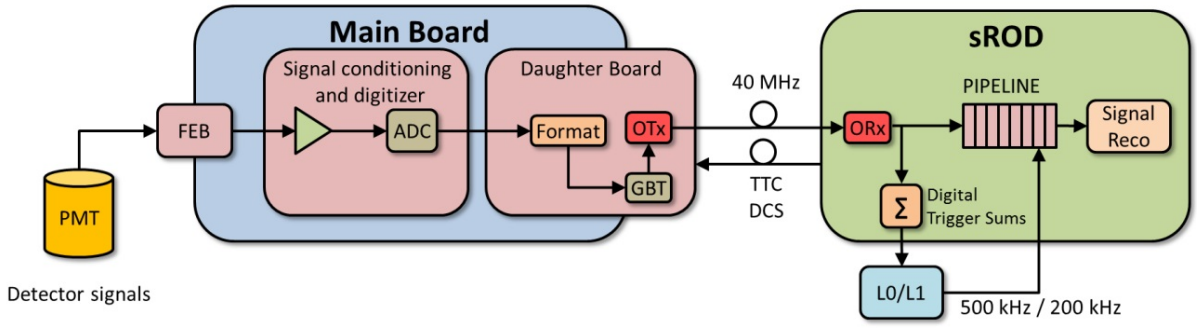


Figure 3: Upgraded Tile Calorimeter readout architecture.

4.1. 3-in-1 Card (FEB)

An improved version of the original 3-in-1 cards was chosen for the FEB in the current demonstrator. Designed by the University of Chicago the new 3-in-1 cards uses modern components allowing for better linearity, radiation hardiness and lower noise [5]. As with

the original design the analog trigger output remained as to be compatible with the present system. The FEBs can be calibrated and monitored via commands sent from the daughter board. Commands can be used to charge and discharge capacitors on the 3-in-1 cards in order to produce calibration pulses used for testing.

4.2. Mainboard (MB)

Each minidrawer [6] in the demonstrator has a Mainboard connected to 12 PMT modules. The mainboard is symmetric on either side such that they will be able to function independently of one another. Each side receives 6 analog PMT signals that are digitised using a 12 bit Bi-gain sampling system resulting in two separate high and low digital signals. An additional output of each FEB is used for the analog integrator with is sampled at 50KHz and read out by a I2C bus. The phase of the signal sampling clocks can be adjusted to compensate for path length delays between MB and DB. All electronics on the MB are commercial off the shelf components. Signals are sent to the DB via a 2 bit serial bus at 560 Mbps. The control and board configuration is done using 4 Altera Cyclone IV FPGAs while the digitisation of the FEB analog signals is done by 12-bit linear Technology LTC 2264 ADCs.

4.3. Daughterboard (DB)

The Daughterboard [7] acts as the interface between the front-end electronics and the sROD. While designing the board major aspects focused on were radiation hardness, high speed readout and redundancy [8]. All minidrawer electronics can be divided in two identical sections: sides A and B. Each side receives data from 6 PMTs and is managed by a Kintex 7 FPGA that is directly connected to the sROD though 10 Gbps optical fibre. In the original front-end design a single Interface board was used to communicate with the ROD for an entire superdrawer.

The 3rd generation daughter board currently used on the Hybrid Demonstrator was developed by Stockholm University. The board uses dual Xilinx Kintex 7 FPGAs, two Quad Small Form-Factor Pluggable (QSFP) optical transceivers and two Giga Bit Transceiver (GBTx) chips. The GBTx chips are used to serialise and de-serialise GBT data streams. The DB is able to communicate directly with the MB through a 400 pin FMC mezzanine connector. The DB receives digitised PMT data through dedicated point-to-point differential signals at a rate of 40 MHz from the MB. The Kintex 7 FPGA then collects the PMT data, formats it and transfers it to the sROD every 25ns. The down-link (sROD to DB) is used to send commands received from Detector Control Systems (DCS) to configure, control and monitor the DB, FEBs, MB and high voltage Board.

4.4. SROD

The Super Read-Out Driver (sROD) demonstrator board [8] forms part of the back-end electronics. Each sROD will be connected to a single superdrawer receiving data from four DBs. The boards primary responsibility will be reception and processing of data received from the detector but will also need to send preprocessed data to the trigger system and act as the interface between the DCS and front-end electronics. The sROD will also implement Trigger, Timing and Control (TTC) functionalities for synchronisation of the read out chain.
The board will utilise a Xilinx Virtex 7 and a Kintex 7 FPGA for its processing needs, four QSFP modules, a send a receive Avago MiniPOD and a SFP mezzanine connector. The Board was built to fit into Advanced Telecommunications Computing Architecture (ATCA) using a double mid-size Advanced Mezzanine Card (AMC).

5. Demonstrator progress

On 9th of June 2014 CERN had a ATLAS TileCal week. During this week the experts from all contributing groups of the Demonstrator prototype came to work on the demonstrator. During

this week four minidrawers were fully assembled and connected together (Figure 4). The week allowed the experts to perform the first tests on a fully assembled superdrawer. A total of 45 PMTs, 4 Motherboards, 4 High voltage Cards and 4 daughter boards were needed to be assembled and connected together. The week was very successful with many new problems being identified as well as confirmation that all the components fitted together correctly and that the entire drawer was able to fit in a slice of TileCal.

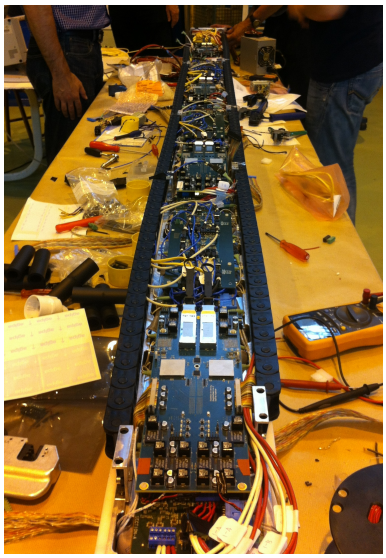


Figure 4: Assembled Superdrawer

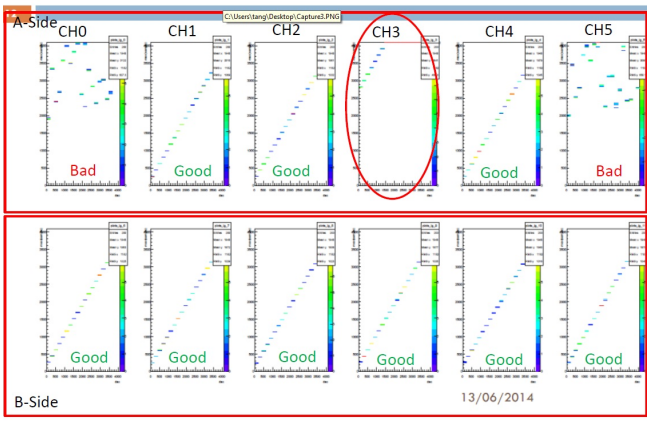


Figure 5: Linearity plots of high-gain channels in mainboard

5.1. Linearity tests

Figure 5 displays linearity plot tests performed on a minidrawer. Here the signal linearity is being checked for the Mainboard high gain channels of one minidrawer. In this test PMTs are turned off and the pedestal setting for each channel are incrementally stepped up. Since there is no signal from the PMTs the plot should be straight line with minor variations due to noise. Due to firmware problems and calibration issues not all the plots are correct. Currently these issues are in the process of being resolved.

5.2. sROD emulator

The sROD described in section 4.4 is still in development and therefore it was not possible for it to be used for the testing of the minidrawers. The demonstrator team therefore have been using a Xilinx VC707 development board to emulate the sROD as an alternative. The VC707 is similar to the sROD in that it also uses a Virtex 7 FPGA. The high speed QSFP connections to the front-end electronics were possible by attaching additional FMC mezzanine modules to the VC707. The Firmware being developed for the emulator could later be modified to be compatible with the final sROD board.

The current setup used for testing the minidrawers has a VC707 board connected to a single minidraw. One problem faced with this testing setup is that a new IP address and/or MAC address is needed for the sROD when the it is connected to a new network. These addresses can be changed by modifying the Firmware but this requires a full firmware rebuild and the reprogramming of the FPGA. To solve this time consuming process a basic interface on the board was created that allows the user to either select a pre-defined address from a list or input a completely new address, all while the board was running. The design uses a LCD module

to display the addresses and four push buttons to act as configuration inputs. The new design saves time and adds a new level of reconfigurability to the demonstrator.

6. Summary

The increase in luminosity predicted after the Phase II upgrade requires a complete redesign of the read-out electronics in the TileCal. The assembly of the Hybrid demonstrator in June greatly assisted with the initial validation of the electronics as well as allowed group members to gain valuable experience. Many more tests still need to be completed and the firmware is still under development but the demonstrator should be ready before the end of LS1.

Acknowledgments

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