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PGAS Model for the Processing Unit of the Upgraded Electronics of the Tile Calorimeter of the ATLAS Detector

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Abstract content
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Advances in new technologies, high speed and more accurate instrumentation for data acquisition, advanced high performance computing technology and better simulation modelling have given rise to the accumulation of massively large amount of data typically referred to as Big-Data.

The ATLAS detector, for instance, operated at the Large Hadron Collider (LHC) records proton-proton collisions at CERN every 50ns resulting in a sustained data flow up to Tb/s. The upgraded Calorimeter will, however, sustain Pb/s of digital throughput. These massive data rates require extremely fast data capture and processing.

Although there has been a steady increase in the processing speed of CPU/GPGPU assembled for high performance computing, the rate of data input and output, even under parallel I/O, has not kept up with the general increase in computing speeds. The problem then is whether one can implement an I/O subsystem infrastructure capable of meeting the computational speeds of the advanced computing systems at the petascale and exascale level. Recent advances in database management technologies are shifting to in-memory (or DRAM) data storage systems since in-memory data processing results in about 100 to 1000X increased throughput.

This paper proposes a system architecture that leverages the Partitioned Global Address Space (PGAS) model of computing to maintain an in-memory data-store for the Processing Unit (PU) of the upgraded electronics of the Tile Calorimeter for high throughtput data processing. The physical memory of the PUs are aggregated into a large global logical address space using RDMA-capable interconnects such as PCI-Express to enhance data processing throughput. Research challenges concern memory-to-memory data copying, fault-tolerance, as well as optimisations for high throughput data processing.

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