Upgrade of ATLAS Tile Calorimeter TTC system for Phase-II test-beam campaigns

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Abstract. The Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS experiment at the Large Hadron Collider (LHC). The LHC Phase-II upgrades will take place during the Long Shutdown 3 period (2026-2028), leading into the High Luminosity LHC (HL-LHC). The HL-LHC will have the capability to deliver up to five times the LHC nominal instantaneous luminosity in 2029. The TileCal Timing, Trigger and Control (TTC) system of the test-beam facility is being upgraded for the Phase-II test-beam campaigns. A new TTC interface module, the ATLAS Local Trigger Interface (ALTI) is being deployed during the Long Shutdown 2 period (2019-2022) of the LHC, as part of Phase-I upgrades. The ALTI is a 6U VME64x module which provides the interface between the Level-1 Central Trigger Processor and the TTC optical broadcasting network, to the Front-End electronics. The ALTI integrates the functionalities of the Local Trigger Processor, Local Trigger Processor interface, TTC VME bus interface and the TTC emitter modules, which are currently used in the experiment. The upgrade involves a new configuration with additional features due to increased amount of programmable logic resources. The status of the upgrade activities is presented.

1. Introduction

The Tile Calorimeter (TileCal) is the central hadronic calorimeter ($|\eta| < 1.7$) of the ATLAS experiment at the Large Hadron Collider (LHC) [1]. It's primary purpose is to provide energy and position of hadrons [2]. The TileCal (shown in figure 1) is constructed with iron plates, plastic scintillators, optical fibres and electronics. It is split into three cylinders along the beam axis, and each cylinder is divided into 64 wedge-shaped modules that are staggered in the ϕ direction. It features one central long barrel (LB) with two partitions (one on A-side and the other on C-side) known as LBA and LBC. The other two short extended barrels (EB) are divided into two partitions, EBA and EBC. The Front-End (FE) electronics are placed within the wedge-shaped modules and are linked to the Back-End (BE) read-out electronics through an optical Timing, Trigger, and Control (TTC) distribution network. The BE electronics control these four partitions through their corresponding TTC crates. The TileCal system performs several weeks of test-beams each year at the CERN SPS North Area in preparation for the ATLAS Phase-II upgrades. The ATLAS Phase-II upgrades will take place during the Long Shutdown 3 (LS3) period (2026-2028), leading into the High Luminosity Large Hadron Collider (HL-LHC). In 2029, the HL-LHC is expected to deliver up to five times the LHC nominal instantaneous luminosity.

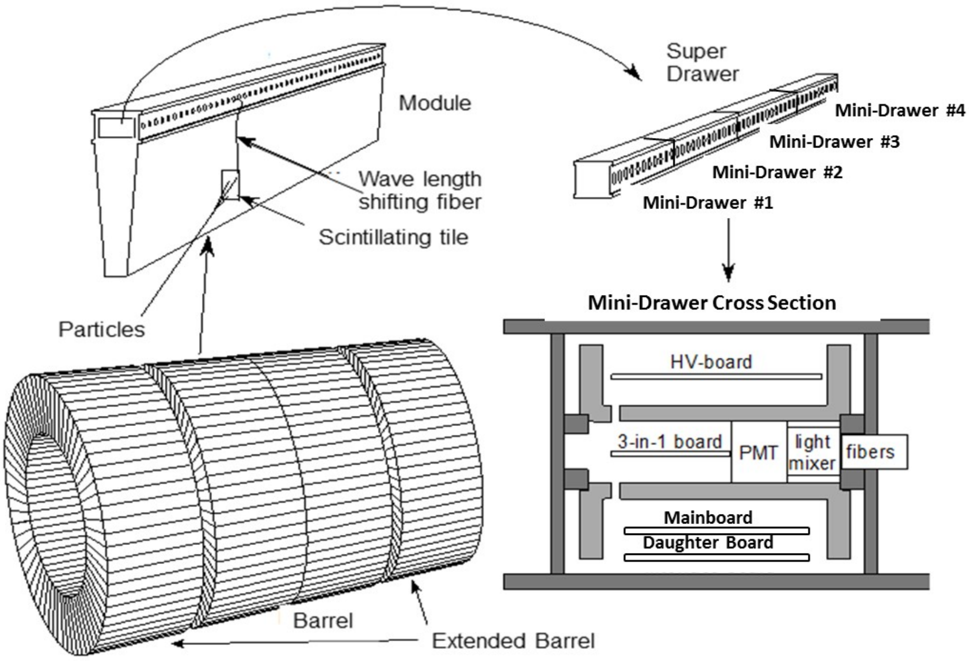

Figure 1: The schematic diagram of the TileCal barrels, showing the module and its components.

An increase in luminosity will result in around 200 proton-proton collisions in every bunch crossing, as well as a large increase in particle flux. As part of the upgrades, the TileCal on- and off-detector electronics will be replaced during LS3. The TileCal data acquisition infrastructure for the test-beam setup is being upgraded with a new TTC interface module, the ATLAS Local Trigger Interface (ALTI).

The TileCal collects data using the ATLAS Trigger and Data Acquisition (TDAQ) system. The TDAQ system selects events with unique characteristics that may be useful for physics analysis. It is built on two levels: the hardware Level-1 and the High Level Trigger (HLT) system. The Level-1 trigger (Level-1 Calo and Level-1 Muon) identifies interesting events promptly based on specific inputs from muon detectors and calorimeters. It uses the Central Trigger Processor (CTP) to lower the acceptable events from 40 MHz (25 ns) to 100 kHz [3, 4]. The corresponding event signal produced by the CTP is known as the Level-1 Accept (L1A). The rate of accepted events is then processed further in the HLT to lower the rate of recorded events from 100 kHz to 1 kHz [3].

2. Test-beam setup at the CERN SPS North Area

The Super Proton Synchrotron (SPS) delivers the test beam-line to the setup. In the beam line, a number of detectors are installed to monitor the beam's quality, position, and particle composition [5]. A schematic diagram of the beam elements used in the test-beam area is shown in figure 2. Three Cherenkov Counters (CCs) are installed to aid in data interpretation and particle identification. As part of the beam trigger system, two trigger scintillators S1 and S2 are also included in the beam line. The beam position is measured with a precision of 0.2 mm using two wire chambers [6]. For muon detection, a Muon Hodoscope is used also known as the Muon wall. It is a mobile detector comprised of 12 scintillators installed behind the Tile modules and is largely used in offline analysis to suppress the pions' low energy tail in high energy hadron runs. The legacy readout electronics are installed in two modules and the Phase-II upgrade electronics are installed in the other two modules. The module configuration changes depending

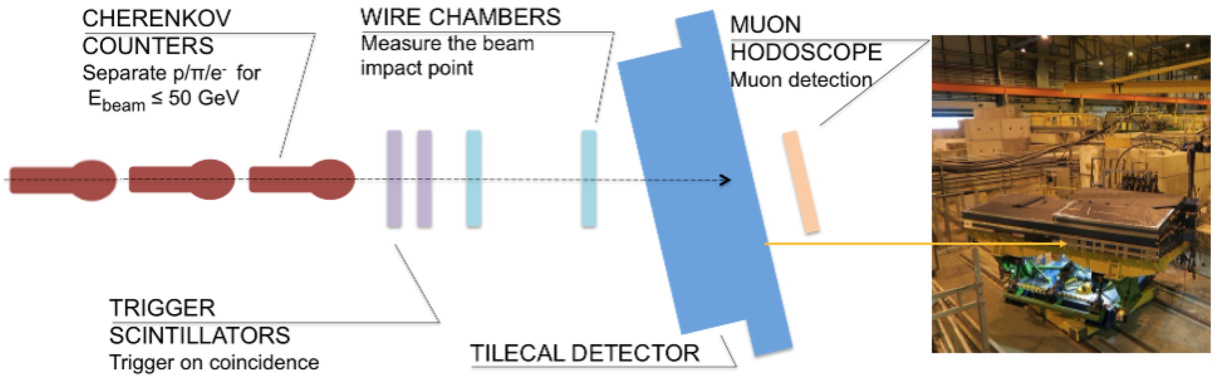

Figure 2: The schematic diagram of the ATLAS TDAQ system, with emphasis on the upgrade of the local TTC system.

on the test-beam program. For interface with the back-end electronics, these modules comprise of Photo-Multiplier Tubes (PMT) blocks with 3-in-1 cards, Digitizer boards, and Interface boards. During test-beams, legacy modules are critical in allowing a comparison between the legacy and new readout electronics. The Demonstrator module incorporates two options: the PMT blocks in the outside minidrawers which are powered by the High Voltage (HV) remote system, while the PMTs in the central minidrawers are powered by the HV internal system. Each upgraded module receives Low Voltage (LV) power from a finger LV power system connected to the module's extreme, and controlled by the legacy detector control system software.

The TileCal modules on top of the scanning table are exposed to low-energy hadrons, electrons and muons in the range of 20–160 GeV. The scanning table is built to rotate the modules at different angles and positions with regard to the incident beam. Data-taking during beam conditions is steered by the DAQ system. The BE electronics are a combination of the legacy and the new upgrade readout electronics. The legacy BE Read-Out Driver (ROD) crate consists of a Single Board Computer, a ROD and a Transition Board Module. The upgrade modules transmit data to two Tile PreProcessor (TilePPr) [1] boards integrated within the legacy TDAQ software through the TTC and ROD interfaces. The TTC system uses the TDAQ software to configure the legacy and upgraded electronics.

3. Upgrade of the Test-beam TTC system with the ALTI board

The ALTI module is a new electronic board designed for the ATLAS experiment at CERN as part of the TTC system [8]. It integrates the functionalities of the four existing modules shown in figure 3 (left), which are currently used in the local TTC system of experiment: Local Trigger Processor (LTP), Local Trigger Processor interface (LTPi), TTC VME bus interface (TTCvi) and the TTC emitter (TTCex). The primary function of the ALTI board is to provide interface between the Level-1 CTP and the local TTC system of the sub-detector. It is made of state-of-the-art components and the logic is implemented in a single FPGA, which allows for more flexibility and added functionalities. During the operation of the detector, the ALTI module receives the TTC signals from the CTP through parallel twisted-pair of low voltage differential signaling cables and distributes them to the sub-detector electronics through the optical TTC distribution network. The full LHC turn consists of 3564 bunch crossings (BCs). The signals received from the CTP are the bunch clock, orbit signal, L1A with 8-bit trigger type and the event counter reset. The bunch clock is the main timing signal produced by the LHC and has

[1] The TilePPr Demonstrator [7] is used to run and read out the Demonstrator module, allowing backward compatibility with the current ATLAS TDAQ and TTC system.

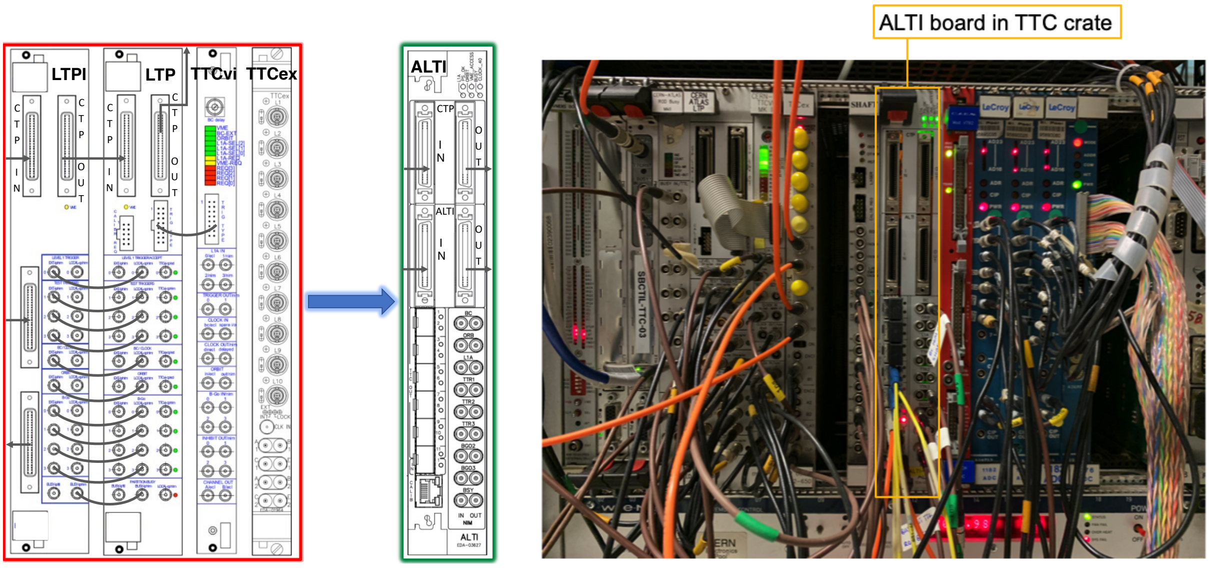

Figure 3: The ALTI module replaces the four legacy TTC modules (left). The ALTI module with new optical fibres integrated in the BE electronics' TTC crate (right).

a frequency of 40 MHz and the orbit signal is the second timing signal that indicates the start of a new LHC turn and allows the identification of the BCs. TileCal ALTI software has been developed, validated and integrated into the Tile online software. The Object Kernel Support (OKS) [2] database for the TileCal test-beam system, has been modified for the ALTI board. The ALTI schema file is loaded in the OKS database and ALTI objects are created from the ALTI classes. In one of the test-beam NIM crates, the beam trigger logic is developed using timer counters, discriminators, and Fan-in/Fan-out modules. When a beam particle creates a signal on the two scintillators, the beam trigger provides a Master trigger signal. The Master signal is then sent to a second NIM crate, which starts the time-to-digital converter measurement of the beam chamber signals and reads out the analog-to-digital converter used for scintillator signal digitization. In addition to generating the Master trigger, the trigger logic sends the L1A signal to the ALTI in the TTC crate, unless the busy signal indicates that the readout path is unavailable. The ALTI then sends the L1A signal to the TilePPr, RODs, and FE electronics.

3.1. Calibration systems and the Diagnostics and Verification System

The updated TileCal ALTI software required an upgrade of the calibration systems [9] as well as the Diagnostics and Verification System (DVS) [10]. These systems have been rigorously tested in relation to the legacy TTC system. To achieve good energy determination and to account for changes in the readout electronics caused by irradiation, ageing, and electronic failures, the TileCal utilizes very accurate and precise calibration systems. The calibration systems are the Cesium system, Laser system, Charge Injection Scan (CIS) and the Minimum Bias System. More details about the calibration systems can be found in refs. [9, 11]. Each system checks a different component of the readout electronics chain and the total calibration of each readout channel is provided by a combination of these tests.

[2] OKS is an object-oriented database with storage based on XML

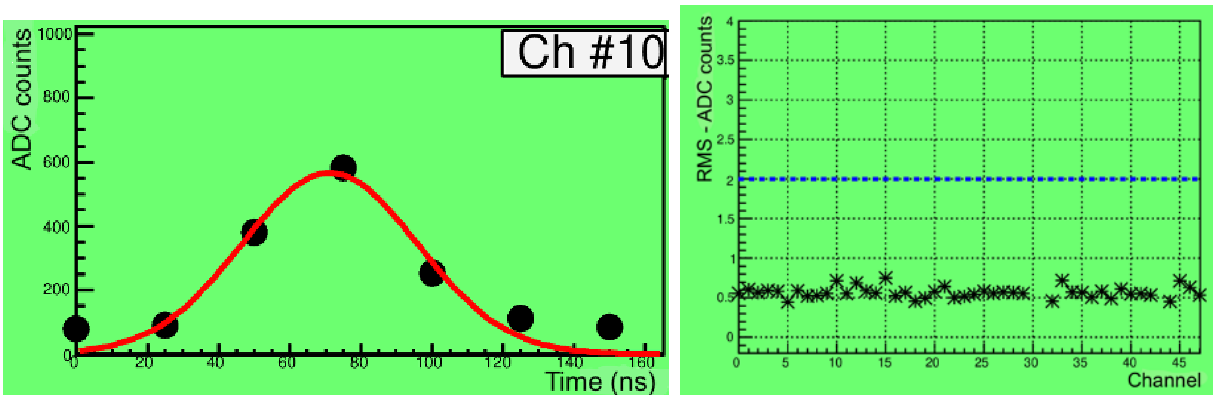

Figure 4: The CIS DVS test performed on one operational read-out module indicates a good reconstructed pulse of the ADC counts versus time for seven samples per channel (left). The RMS ADC counts versus the channel number are shown in the pedestal DVS test, and the electronics noise level is below the threshold for all read-out channels (right).

4. Results

Calibration and DVS results are performed to validate the new TDAQ system using the ALTI board. Seven samples are produced when the DAQ system is well calibrated, the samples result in a Gaussian fit for pulse recognition. The DVS tests are used to check for the digital readout of the super-drawers, and are performed for CIS as shown in figure 4 (left) and Pedestal as shown in figure 4 (right). CIS results show a good pulse shape resulting from good signal reconstruction. Pedestal results show that noise levels are within acceptable levels for module LBA01.

5. Conclusions

Several test-beam campaigns are conducted at the CERN SPS North area in the Prévessin site, to evaluate the TileCal Phase-II upgrade electronics for the HL-LHC project. There are usually two test-beam periods during the year and each test-beam period takes two weeks, with access to the beam line. Data is collected, with Tile modules being sampled with varying energy beams and positioning to the beam line. The TileCal TTC system has been successfully migrated to use the ALTI board. Calibration and DVS results to validate the TDAQ system are shown, in preparation for the upcoming test-beam campaigns using the ALTI system. Results for the first test-beam campaign using the ALTI system, showing the distributions for kaons, pions, and electrons, will be obtained in November 2022.

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