

ATLAS Tile Calorimeter Phase-II upgrade low-voltage power supply production and testing

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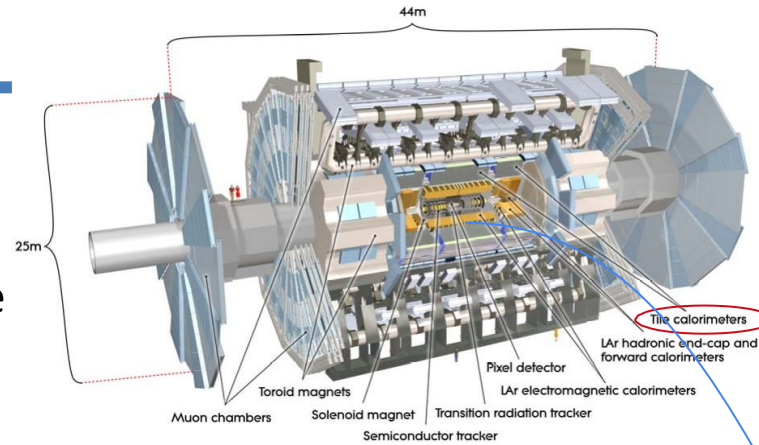


**National
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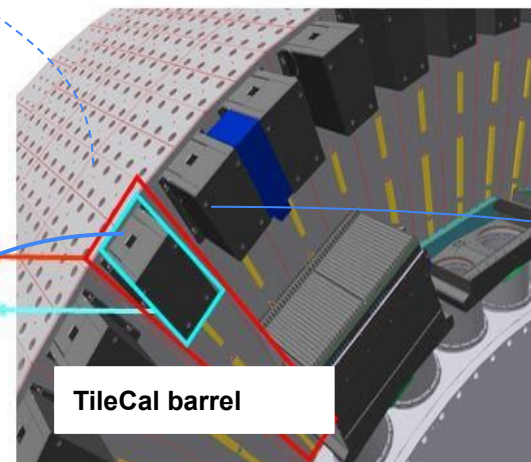
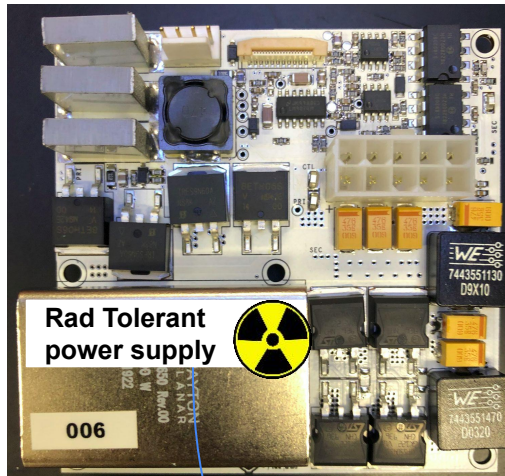
Context

- **256 modules** in detector, **~10,000** readout channels.
- **Iron** as absorber and **plastic scintillator** as active material.

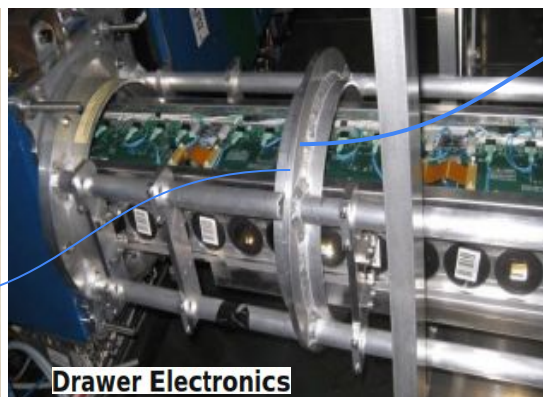
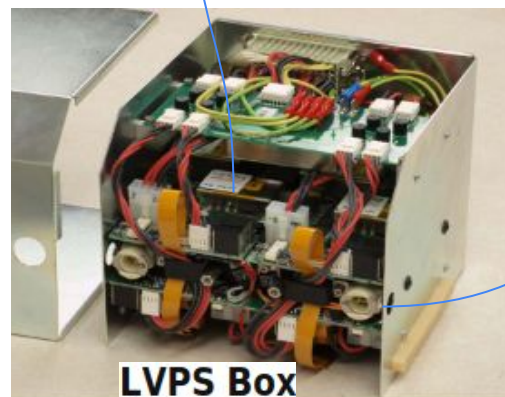
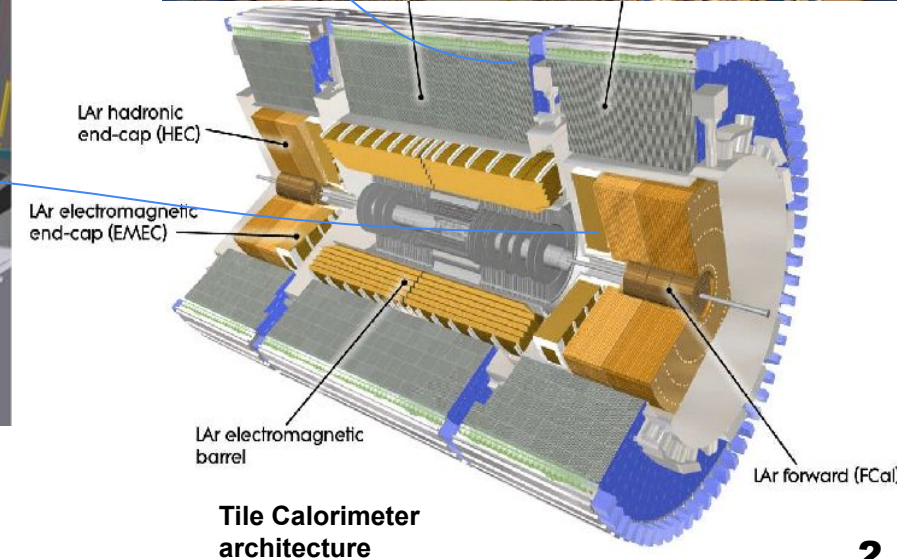
SA contribution: 50% for TileCal



ATLAS detector



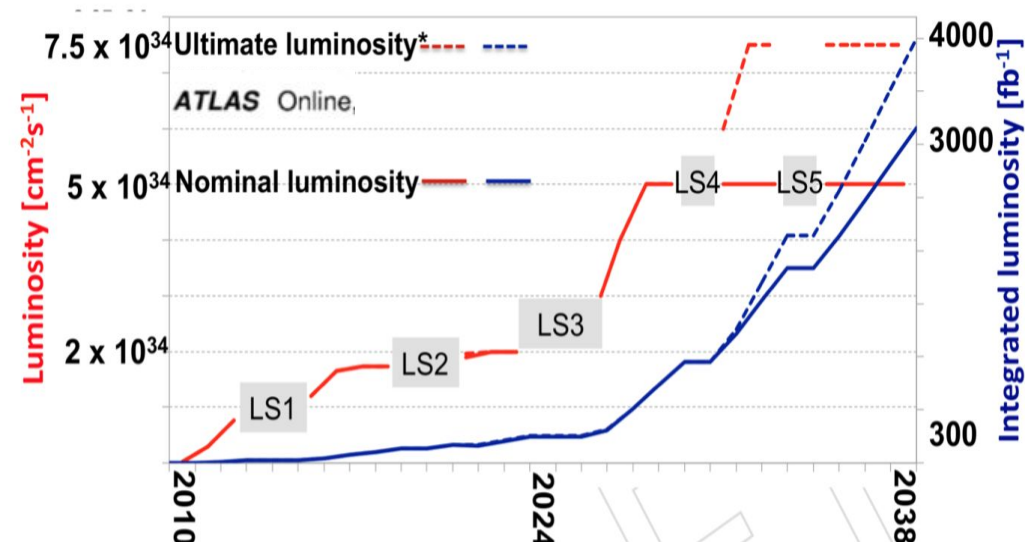
Tilecal: one barrel (6m), 2 endcaps (3m).
- 256 drawers with front end electronics.
- 256 power supplies, 300W each.



TileCal LVPS Redesign Project

Redesign project

- Community working on replacing all readout electronics because of long-term reliability with increased luminosity
- Involves replacing all electronics and increasing the radiation hardness for handling a maximum total integrated radiation dose ~ 400 Gy of TID, 4×10^{12} n/cm² of NIEL and 2.5×10^{12} p/cm² of SEE estimated over 15 years of operation.
- Require efficient, low-ripple, stable and reliable with the increased luminosity



Features:

- Customly built, compact,
- Water cooled using Al_2O_3 components ;
- 10 V Bricks, 2.3 A
- Environment: Magnetic field; Radiation tolerant
- Efficiency target: 75%

Reliability is important, difficult access to detector!

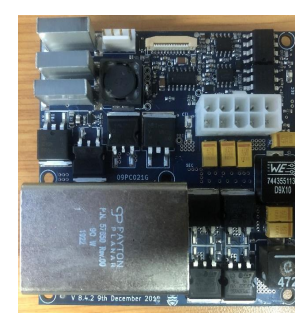
Original Bricks to latest design



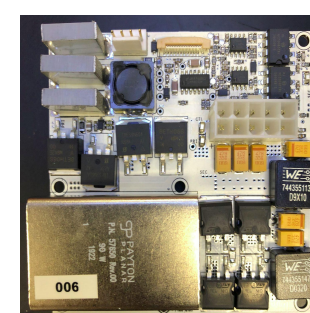
6.5.1 Original Brick



v 7.5 ANL brick



Old 8.1.0 WITS Prototype



Latest WITS Prototype 8.4.2

- ATLAS Tile Calorimeter Phase-II Upgrade Technical Design Report : <https://cds.cern.ch/record/2302628/>
- Upgrade of Tile Calorimeter of the ATLAS Detector for the High Luminosity LHC Journal of Physics, DOI:10.1088/1742-6596/928/1/012024,2017.

Power and Read out Architecture

Number of power stages that will do the job?

- Upgrade from a **2-stage to 3-stage** power powering system distribution system to accommodate the FE upgrades.

- Front-end power supplies all $\pm 10V$

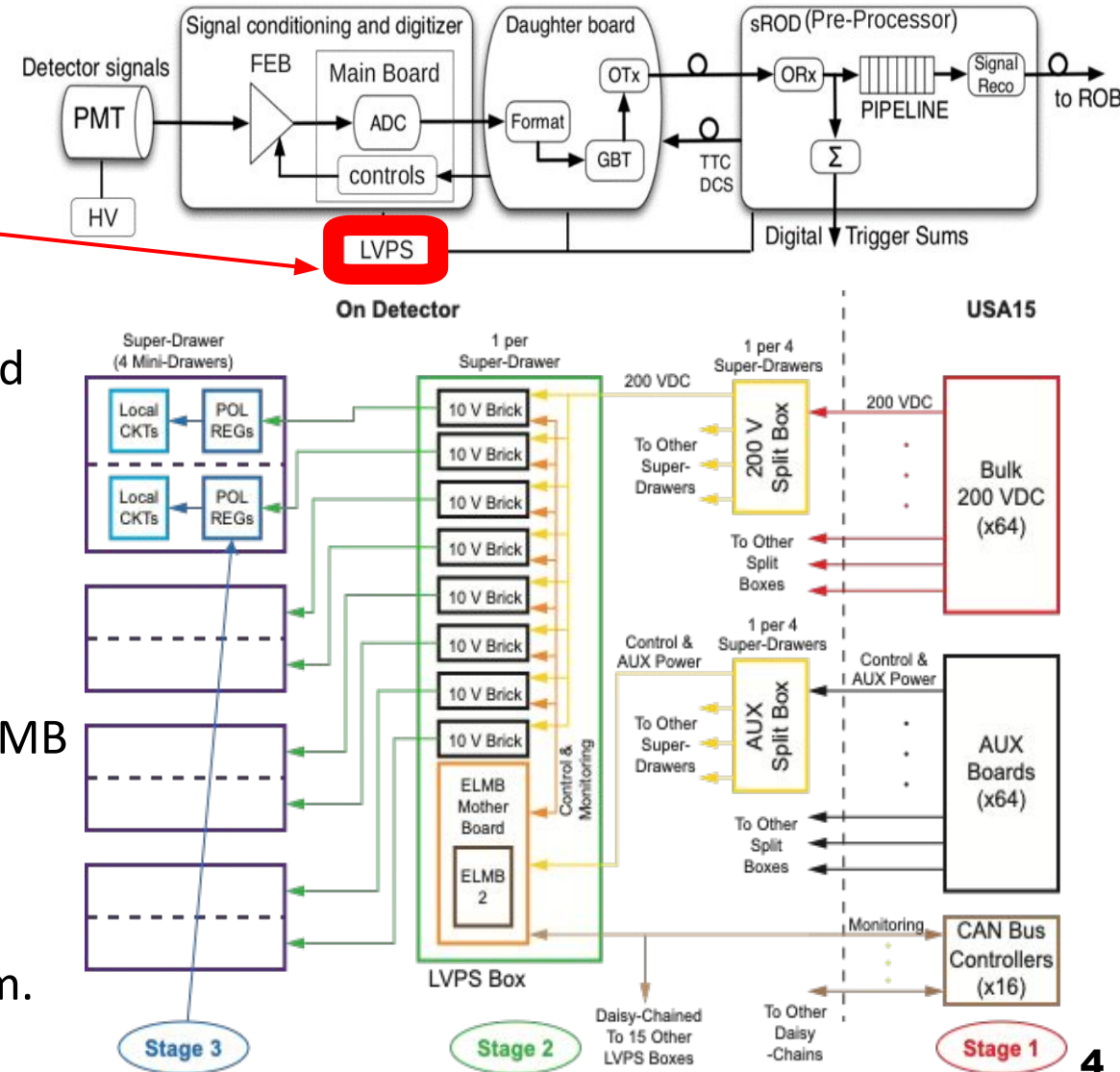
- New: Point-of-load regulators

- Converts **200 V DC** to **10 V DC** to provide power to front-end electronics.

- All eight power supplies have the same **specifications** and **performance** requirements.

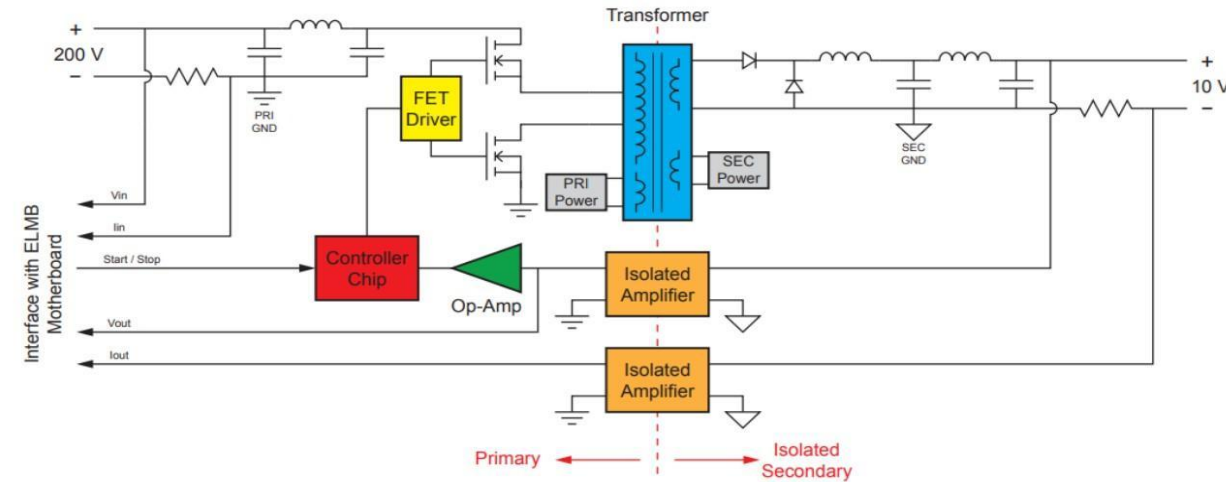
- LVPS monitoring system is still in progress but will utilize ELMB (**Embedded local monitoring board**) for control and monitoring of individual brick.

- LVPS's represent a **single point failure** in the readout system.
i.e. – loss of data from a module.



Brick principle of operation

- Transformer coupled buck convertor (Forward converter).
- Controller chip **LT1681** (*Heart of design*) is used to provide switching at frequency of ~ 300 kHz
- FET's: When conducting current flows to the primary windings of the transformer which transfers energy to the secondary windings.
- Opto-Isolators: Provide voltage feedback.
- Shunt Resistor: For measuring the output current.
- Protection circuitry: Overcurrent Protection , Over Voltage Protection, Over Temperature Protection.



| Parameter | Value |
|-----------------------------|----------------|
| Threshold for Stable Load | < 2 A |
| Over Voltage Protection | 11.5 – 12.5 V |
| Overcurrent Protection | 6.75 – 10.75 A |
| Output Voltage Ripple @ NL | < 0.5 V (p2p) |
| Duty Cycle @ NL | 30 – 40 % |
| Frequency @ NL | 280 – 320 kHz |
| Efficiency @ NL | > 65% |
| Input Power (Current) @ NL | 48 W (0.24 A) |
| Output Voltage Change | < 20 mV/A |
| Over Temperature Protection | 70 Degrees C |

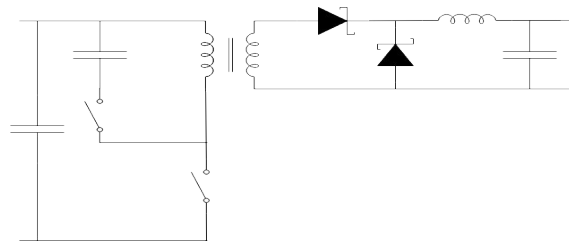


Talk to Experts (again); Look at datasheets of similar products



Compile your list of required specifications

From Topology to Components



Power Topology

Simulation
Calculation

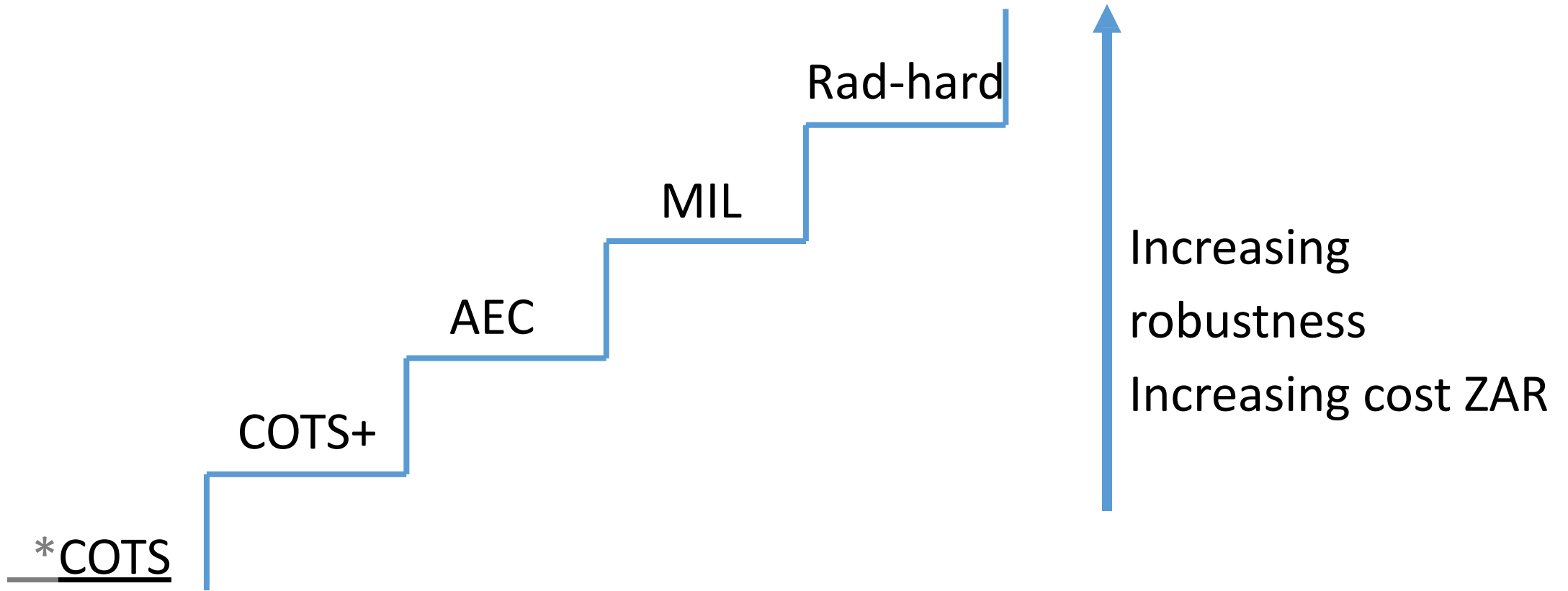
Radiation Tests
Custom Magnetics
Other Modifications

Get ALL waveforms (v, i)
Get ALL losses (p)

Choose active and passive components

Premise

COTS = COST Advantage

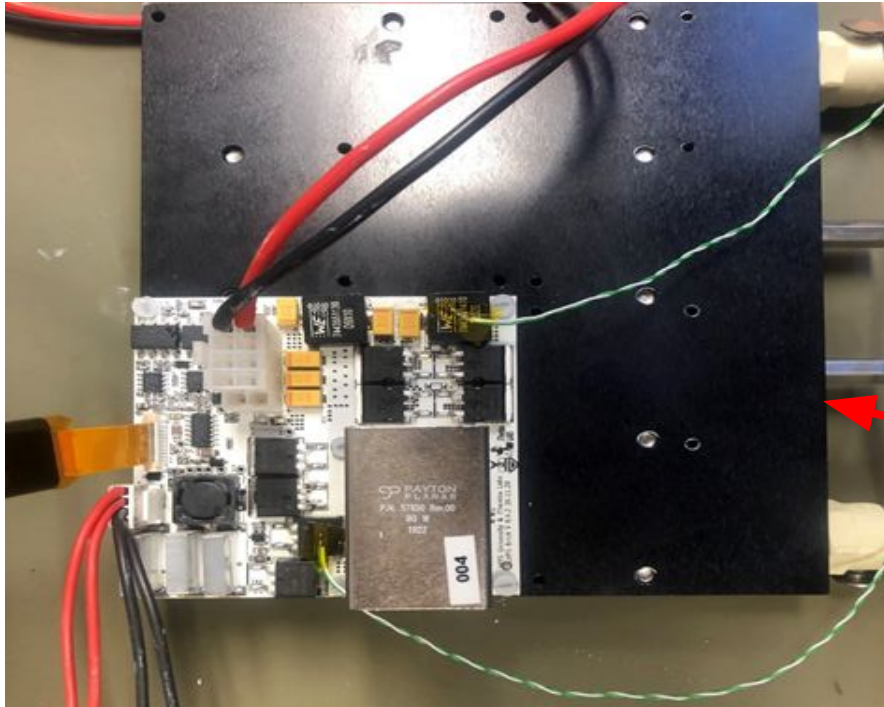


*Commercial Off-The-Shelf

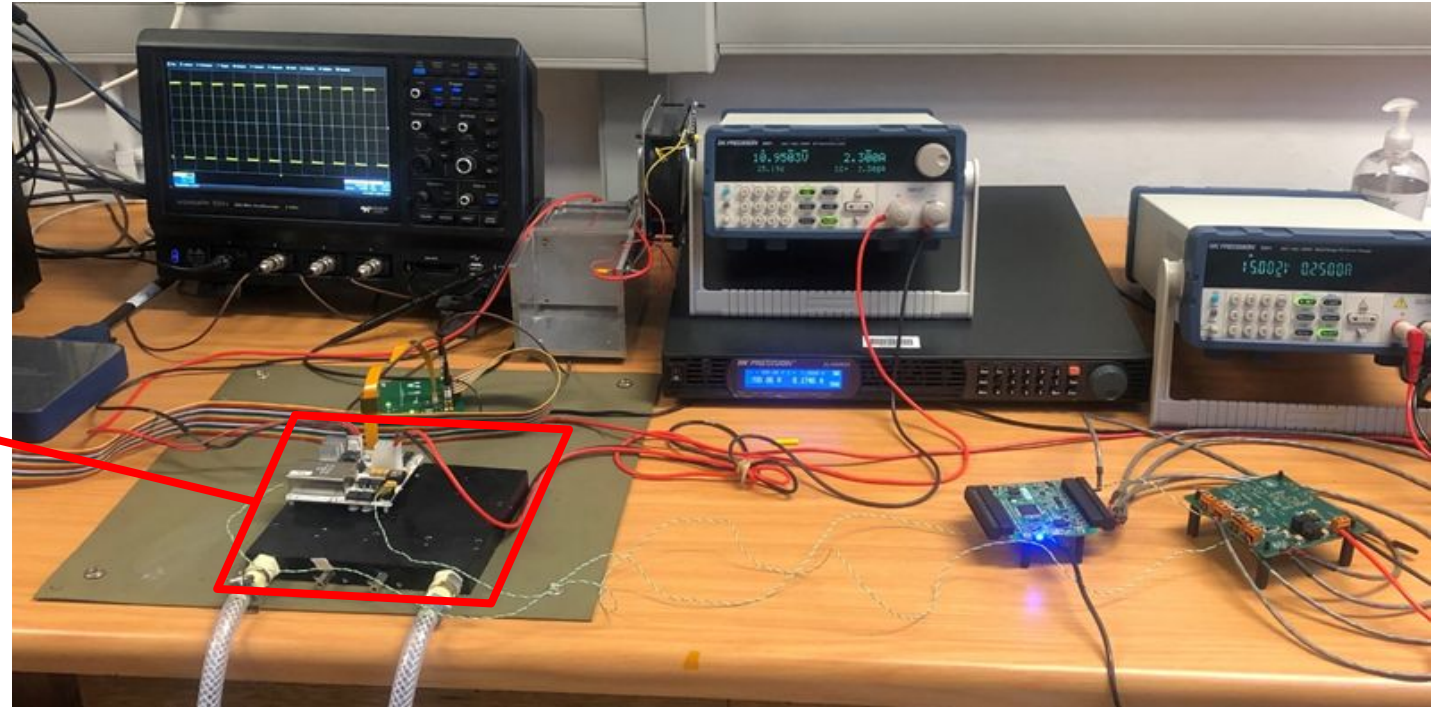
Testing of prototypes at Wits

- ❑ Test setup comprises of a single brick test stand running on one cooling plate coupled by custom temperature test set up to monitor the temperature of the components on top of the case to observe component characteristics as they vary with temperature.
- ❑ Test bench based on computer controlling and reading out equipment which perform the tests in LabVIEW

HE brick on cooling plate

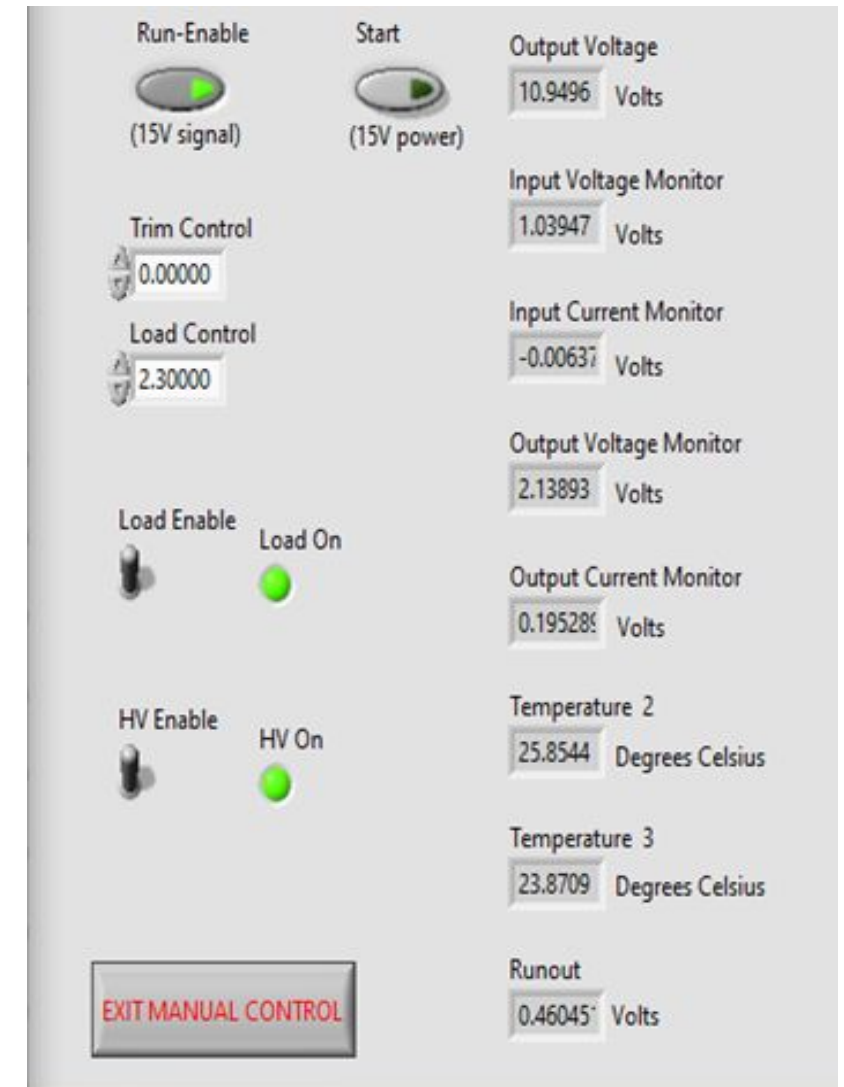
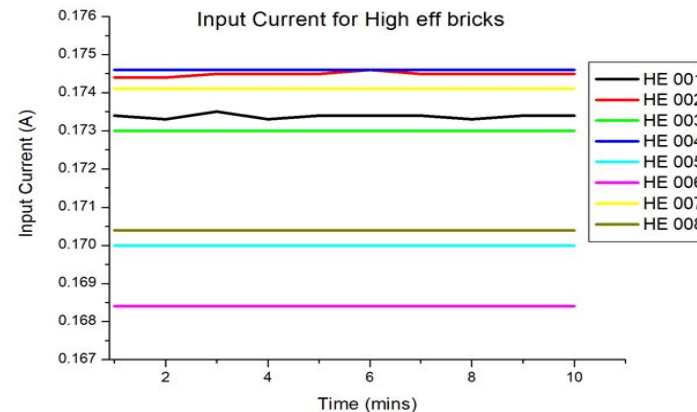
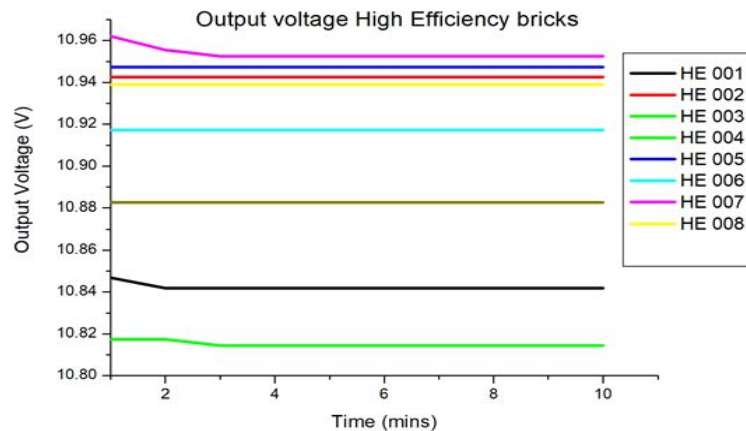
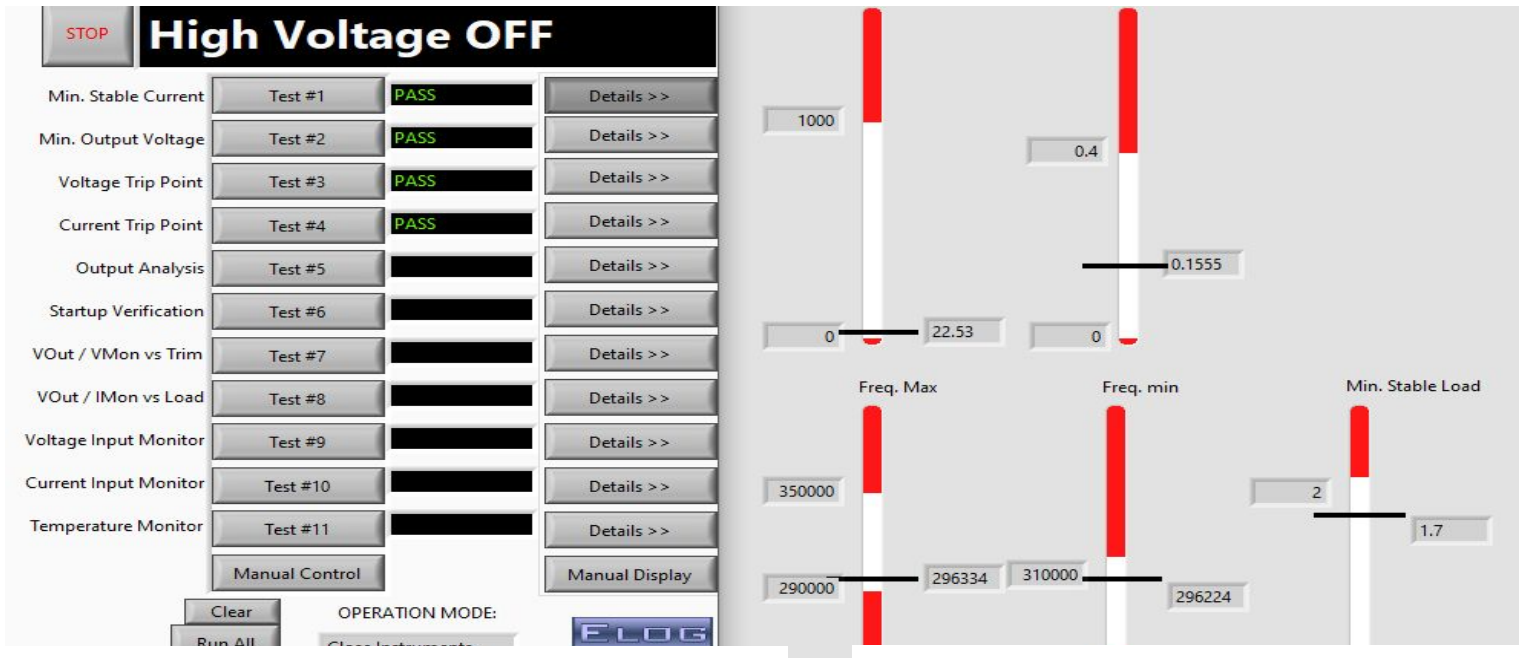


WITS brick test stand



Testing of prototypes at Wits

- Bricks were tested and monitored for ~15 minutes on 18/19 Sept '21, and all 8 bricks managed to start without issues.



Brick Improvements thus far

Critical Issue: Thermal Management

⇒ **The symptoms:**

- Brick experienced high temperatures during operation
- *U1 (controller chip) & U2 (FET driver) had high failure rates*

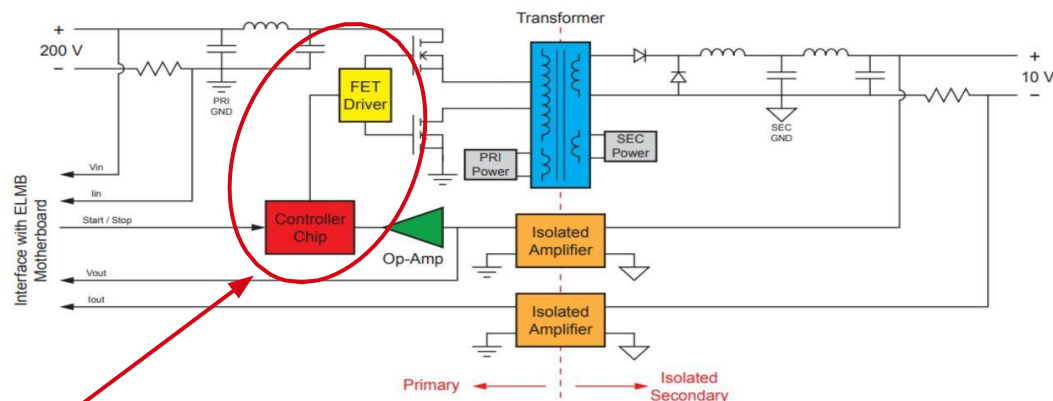
⇒ **A possible cause:**

- *Insufficient thermal coupling to cold plate*

⇒ **What we did:**

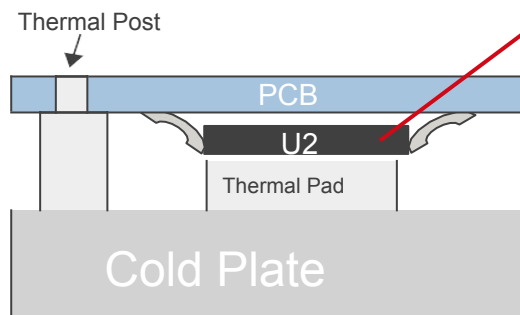
- **New Higher efficiency MOSFET used (To be rad validated). Locally produced Al₂O₃ (aluminum oxide) ceramic cylinders used**
- **Add thermal Bergquist (Gap Pad) to couple chips to cold plate**

Brick Block Diagram

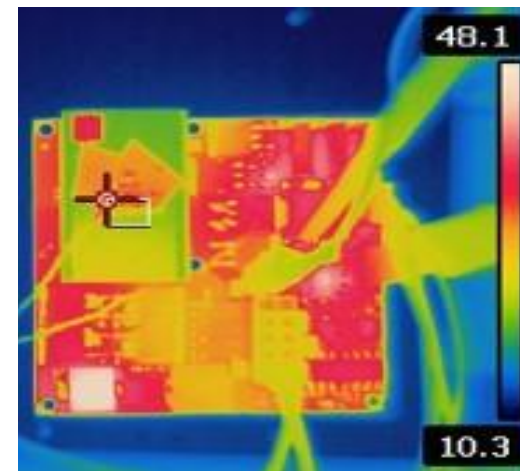


*See Othmane Moune's talk

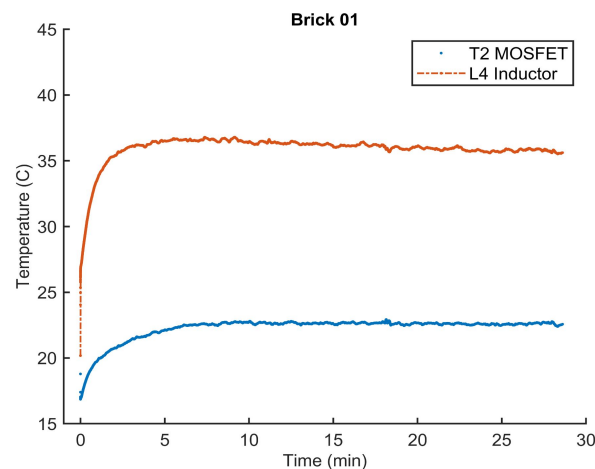
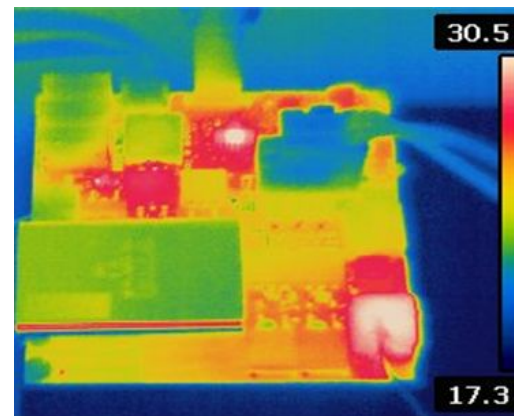
Implementation







Older v8.1.0 WITS brick



New Version 8.4.2 WITS brick



Summary

-  Re-design of power supply project on track and identified isolation amplifier to be replaced
-  For pre production run, active components have been already procured, passive components still to be ordered
-  Some components active components are pending finalization of radiation test requirements
-  Looking forward to start of Pre-production late 2022

Supported by:



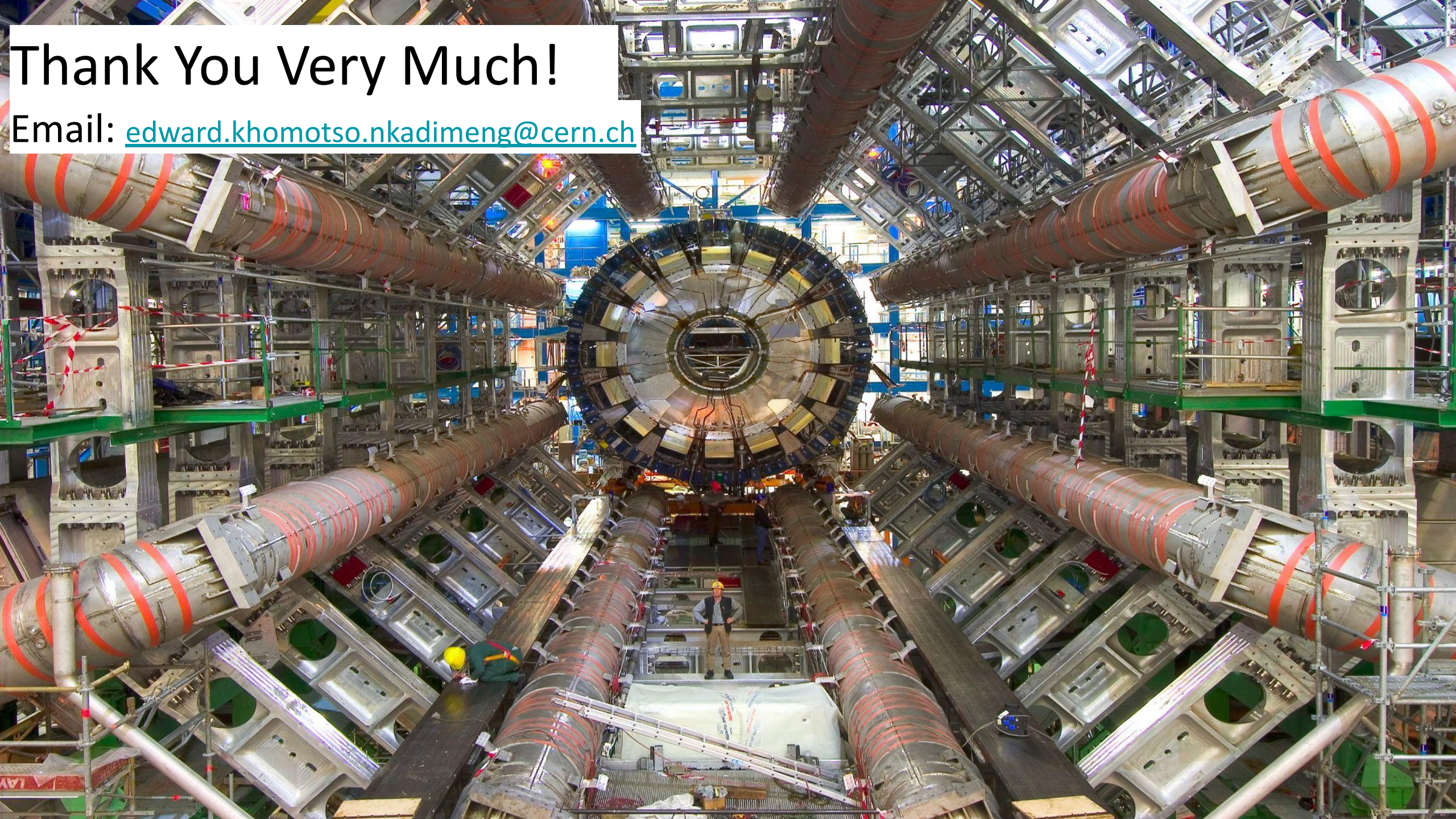
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National
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Foundation

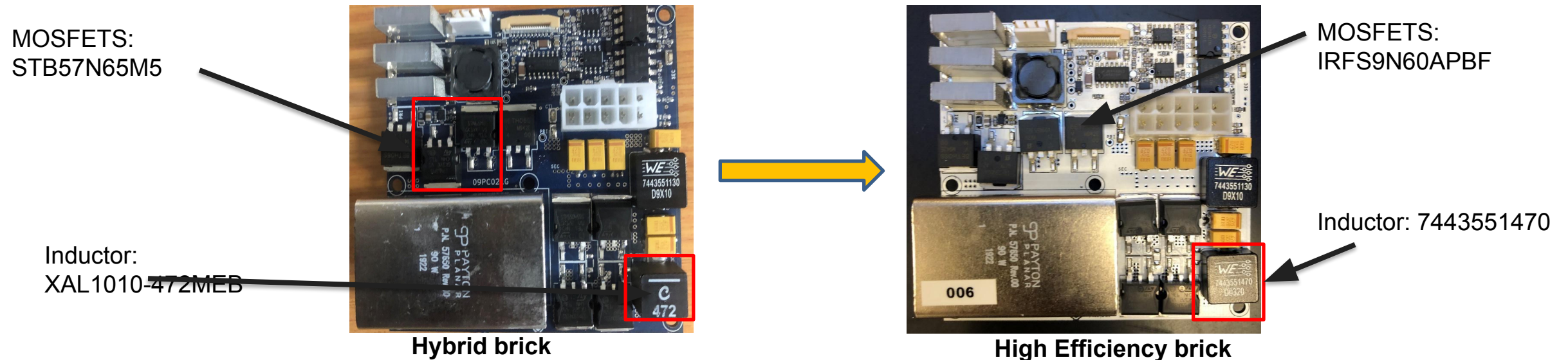
Thank You Very Much!

Email: edward.khomotso.nkadimeng@cern.ch



Latest brick production at WITS

- ❑ PCB design v8.4.2 was used for the latest round of eight (8) bricks populated in SA.
- ❑ Design changes include a different output inductor (736-2037, Würth, WE-HCI,) and different MOSFET (RFS9N60APBF) as was identified in thermal testing undertaken at CERN, showed a brick efficiency increase from 55-60 % to 68-75%. (**component still to be rad certified!**)
- ❑ 14 thermal posts per brick used for heat transfer from components to the cold plate from which 8 are metalized and 6 non-metalized. For the latest iteration eight (8) bricks populated using purely Al₂O₃ ceramic cylinders.



Latest brick production at Wits and pre-production plans

- ❑ Eight bricks were assembled in May, 2021 and were inspected and tested at WITS using the individual brick test stand and a custom temperature before being shipped to CERN.

Pre-production preparation (104 bricks):

Halogen Free PCB's:

- ❑ Option of TU-862 HF (High Tg) Material and in contact with PCB supplier

Stock parts

- ❑ Active components ordered, Passive still to be ordered
- ❑ Add. LM9074 ~1700 parts ordered

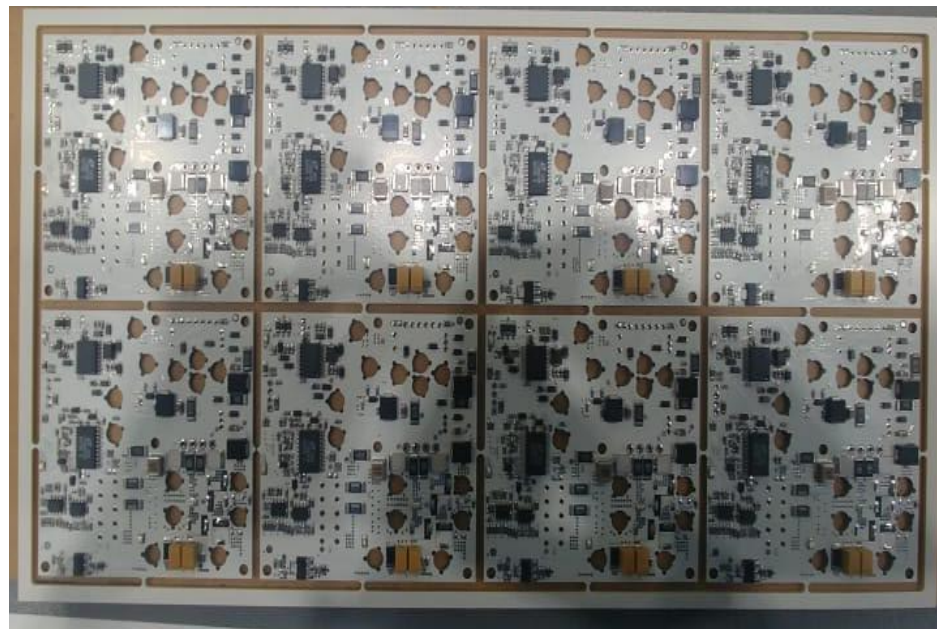
Transformers

- ❑ Awaiting delivery of 104 transformer pieces and setting up order for 1032

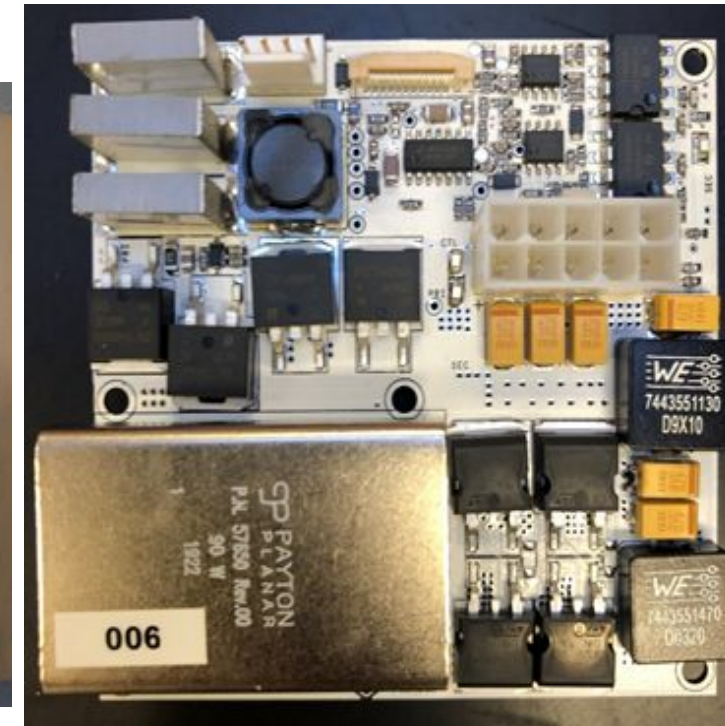
Ceramic posts

- ❑ Ordered 15000, PO issued

LVPS panel component assembly



LVPS brick



LVPS Thermal results

- ❑ Temperature 2 and 3 data measured every minute interval from available brick thermistors.
- ❑ Preliminary temperature results using new high efficiency MOSFET show a significant temperature reduction in all bricks by almost $\sim 10^{\circ}\text{C}$.

v 8.1.0

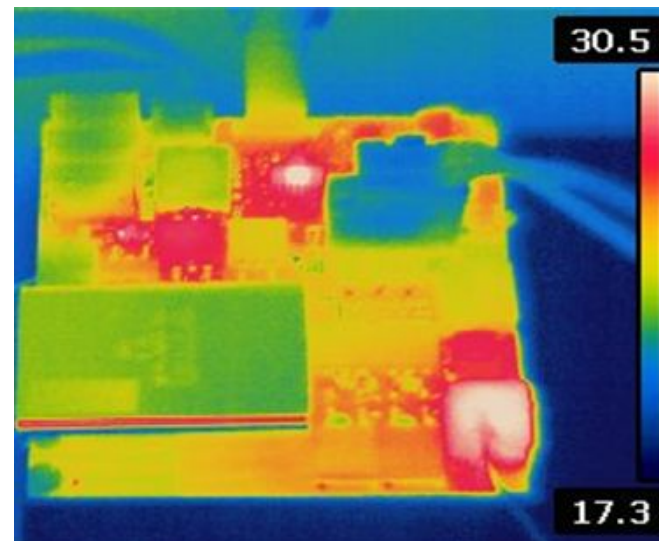
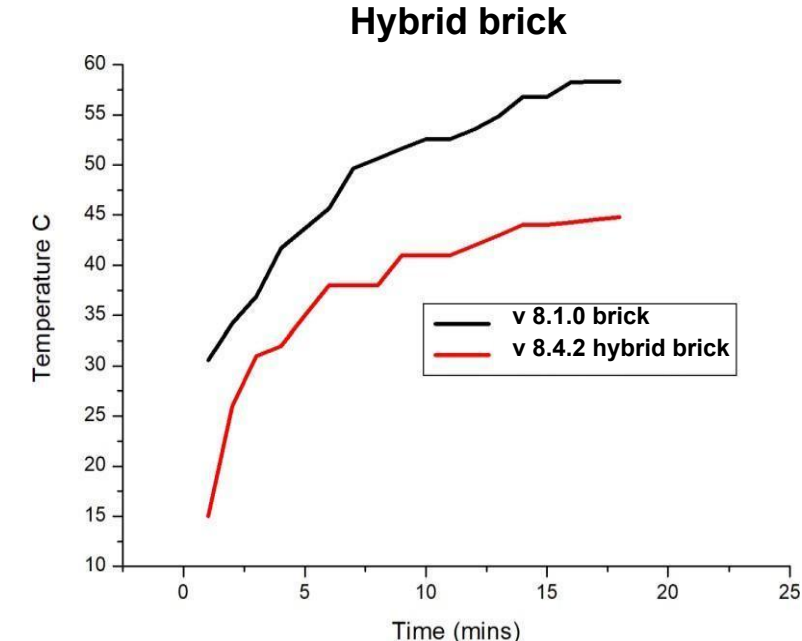
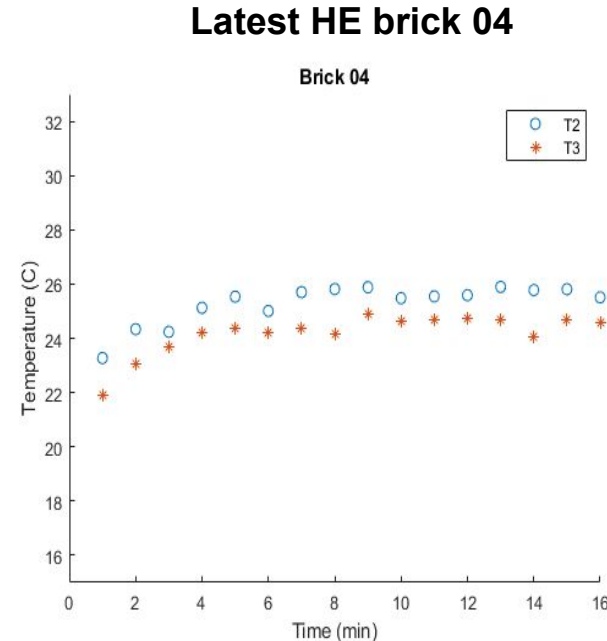
- Avg Temp 2 $\sim 50.4^{\circ}\text{C}$ and Temp 3 $\sim 39.1^{\circ}\text{C}$

v 8.4.2 hybrid bricks (AlN and AL2O3 posts)

- Avg Temp 2 $\sim 38.2^{\circ}\text{C}$ and Temp 3 $\sim 31.1^{\circ}\text{C}$

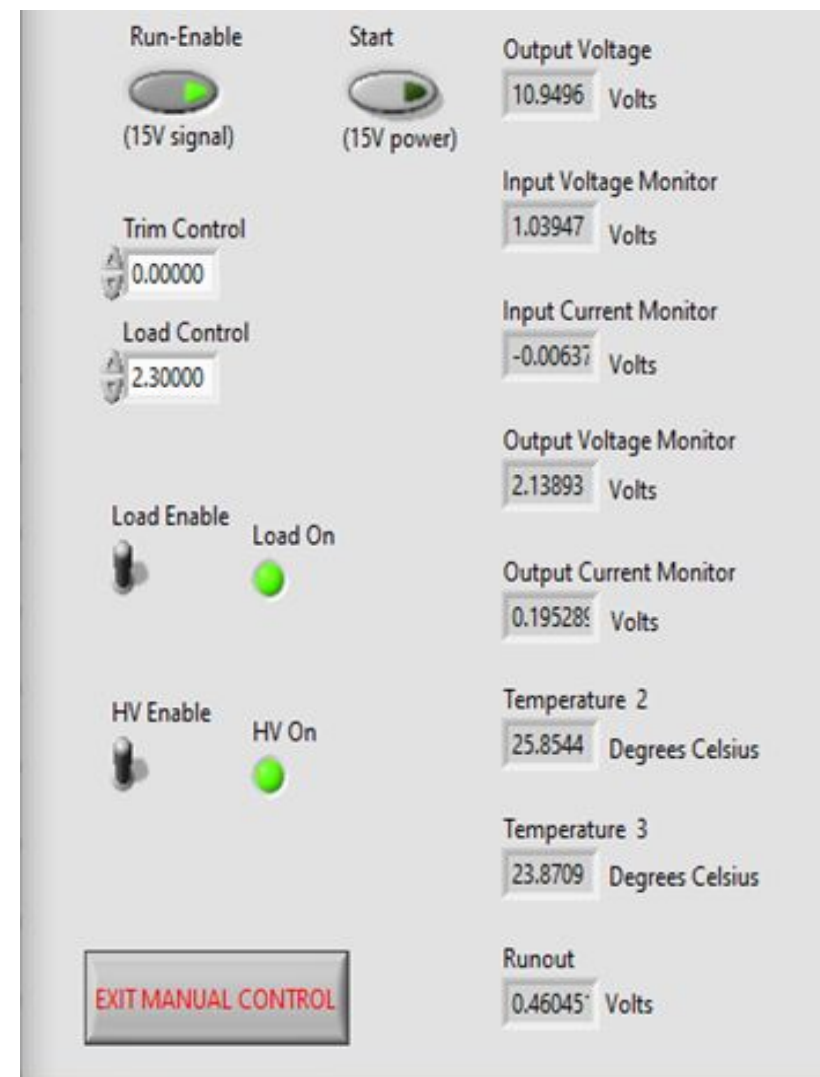
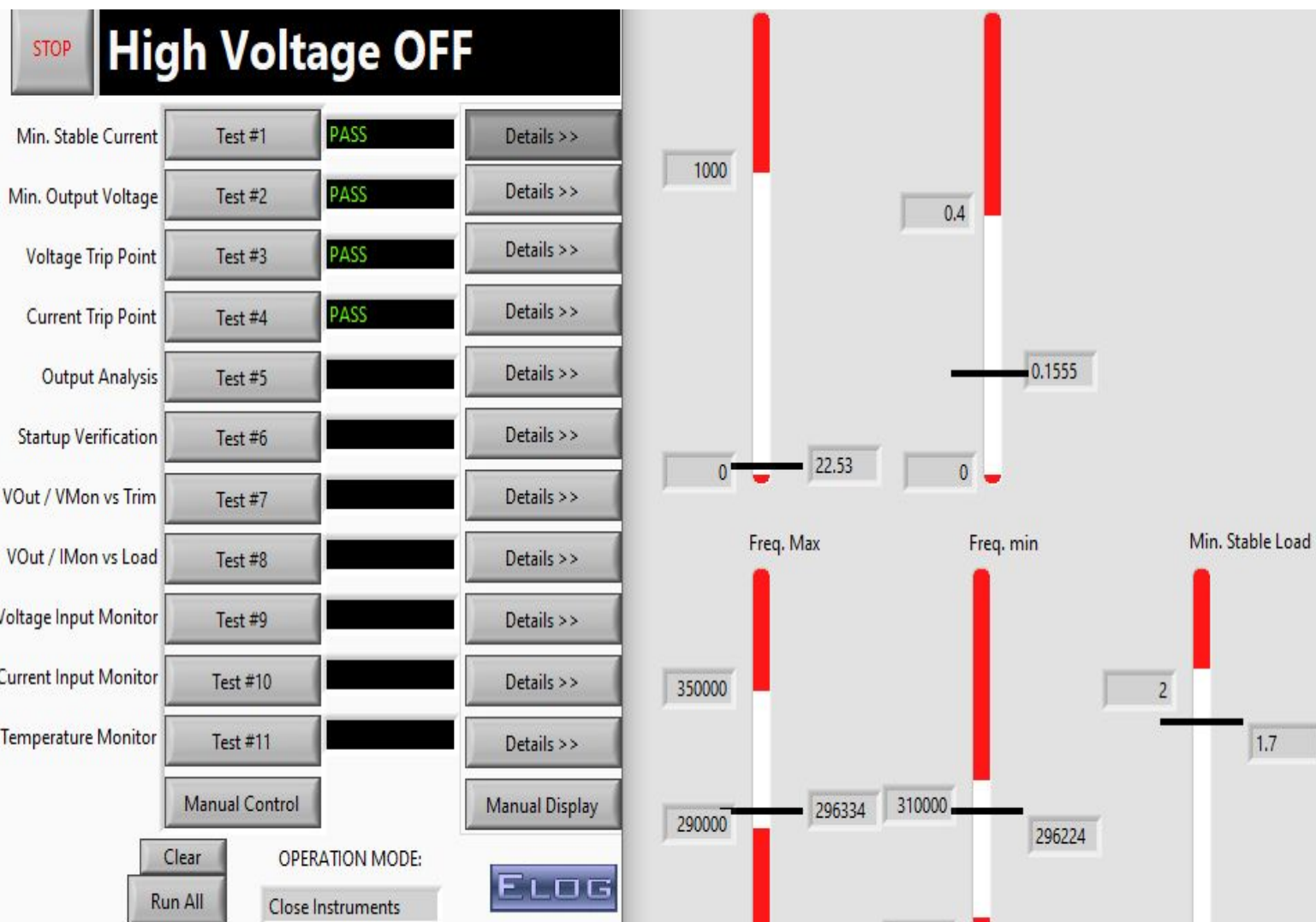
Latest v 8.4.2 (purely Al2O3 posts+ HE MOSFET)

- Avg Temp 2 $\sim 27.2\text{-}29.0^{\circ}\text{C}$ and Temp 3 $\sim 24.1\text{-}27^{\circ}\text{C}$



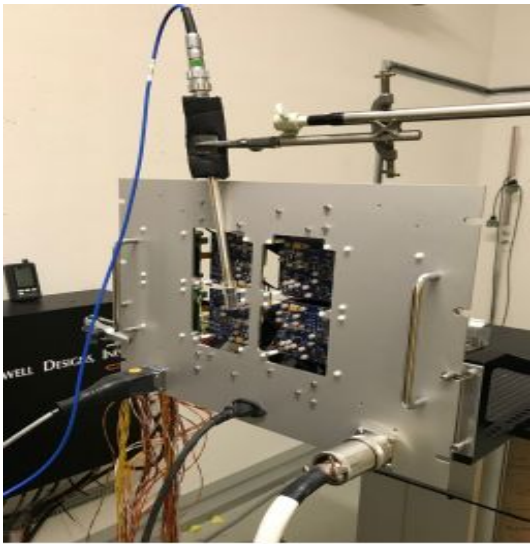
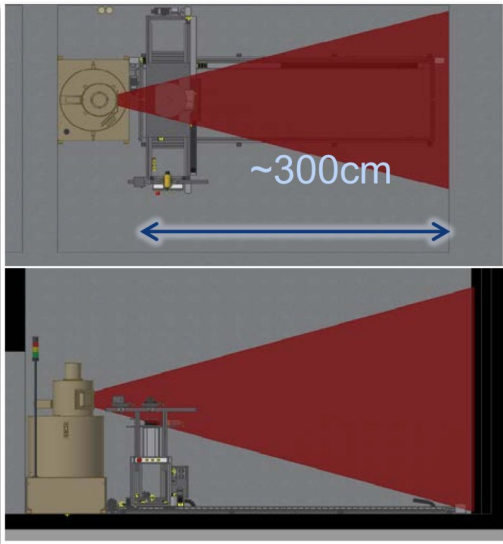
Testing of prototypes at Wits

- Bricks were tested and monitored for ~15 minutes on 18/19 May '21, and all 8 bricks managed to start without issues.

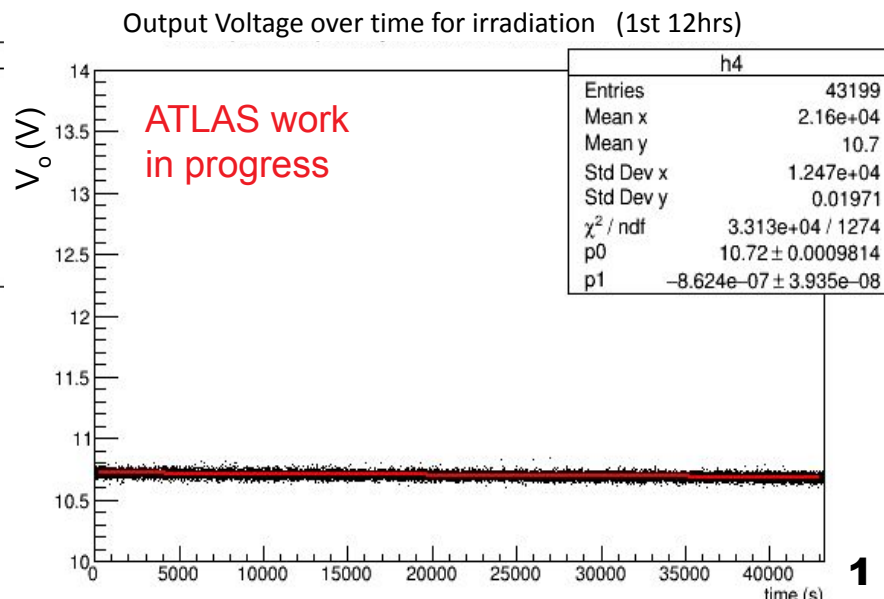
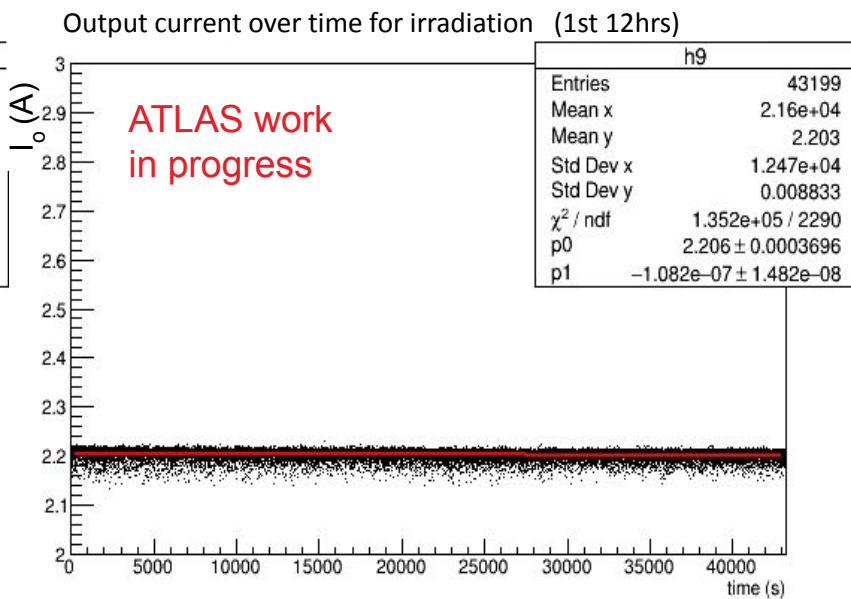
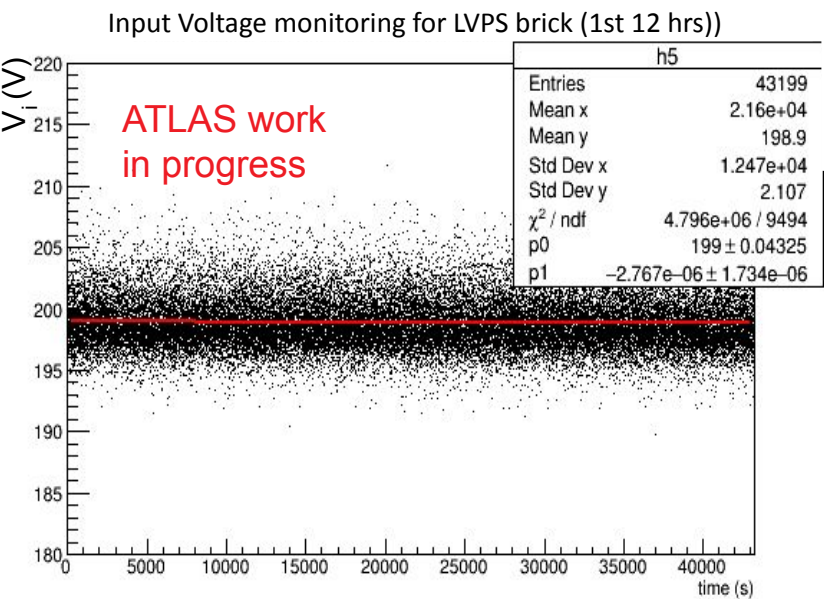


Radiation testing results: Gamma (CC60 Facility)

- ❑ We tested 8 bricks up to a target dose of close to 500 Gy.
- ❑ All the 8 bricks were running monitoring during up to end of the tests with only an output voltage drop of 1 mV/Gy.
- ❑ This drop is completely acceptable due to wide range of input voltage for our front end electronics.
- ❑ Parameters show expected behaviour as a function of time.



TID tests of LVPS boards in CC60 facility

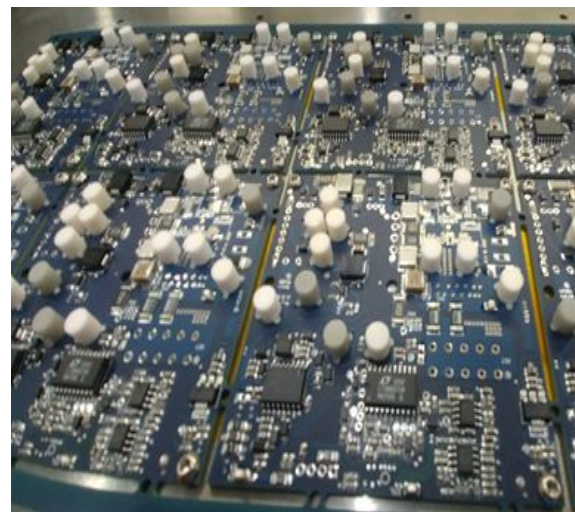


Brick Improvements thus far

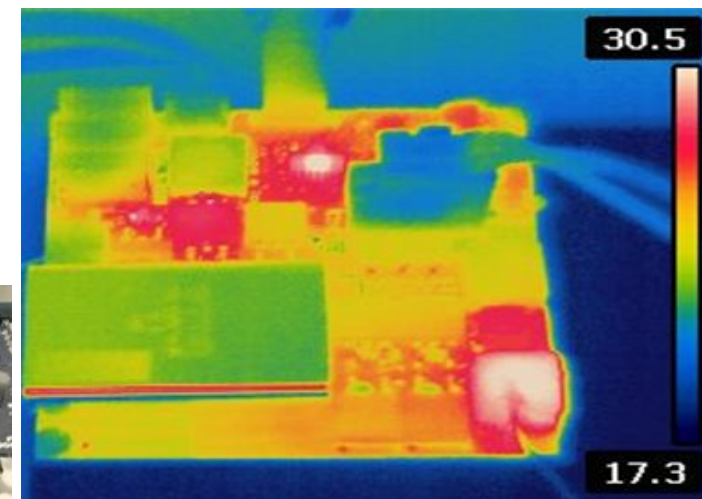
Improved
Reliability

- **Critical Issues**
 - HF Printed circuit boards
 - Reliability studies conducted
 - Better thermal management (Still to be rad validated)
 - Better ESD protection of ICs and Capacitor
- **Medium-Impact Issues**
 - Improved stability
 - Improved trip circuitry
 - Power sequencing
 - Fabrication and soldering quality from supplier
- **Low critical but desirable**
 - Start-up pulse current
 - Improve monitoring circuitry
 - Reduce/improve tuning for final output Voltage

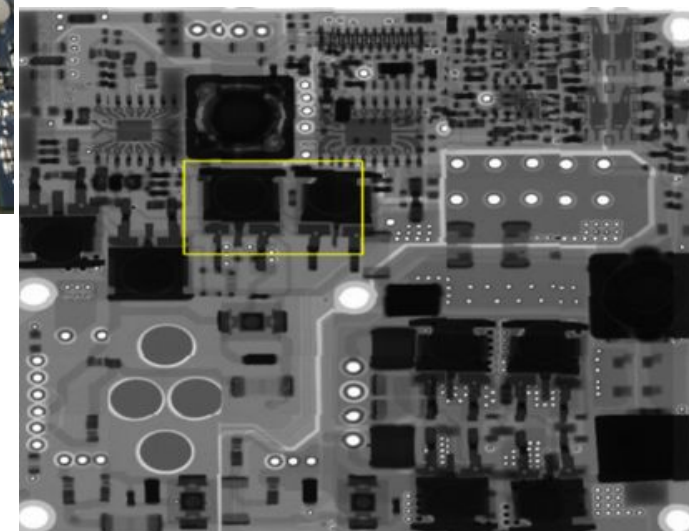
Population of power supplies



Thermal Image

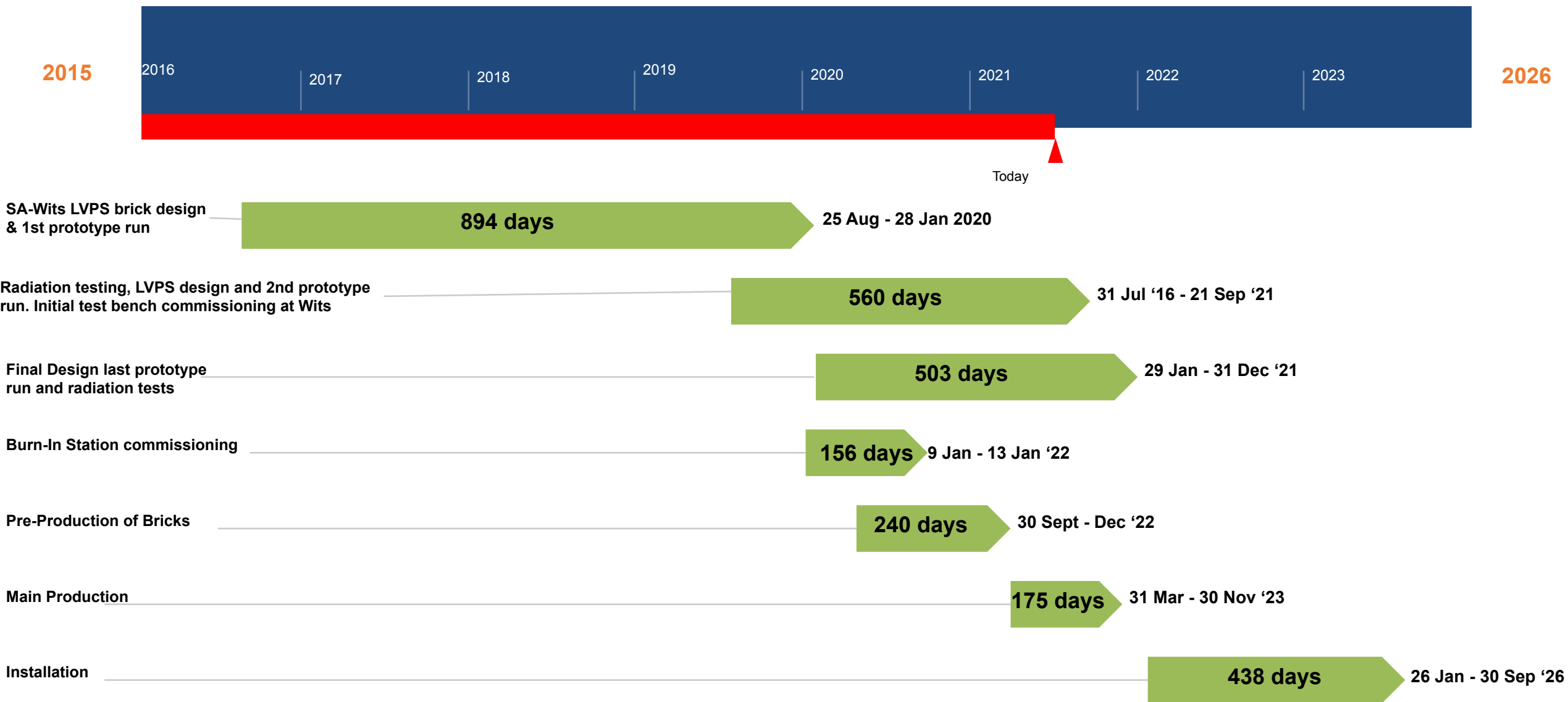


X-ray Inspection technology



Improved
Performance

Schedule for LVPS project in SA



Radiation Criteria: ATLAS Radiation Policy

- ❑ **ATLAS Extraction Tool** enables to locate the highest irradiated area, close to the edges of the Tilecal Long Barrel
- ❑ Safety factors are introduced by the ATLAS Electronics Coordination Group as specified in Table below to account for error margins associated with the different types of radiation tests.
- ❑ Safety Factors: SF_{sim} (Safety Factor on the simulation giving the Doses or Fluences) and SF_{lot} (Safety Factor corresponding to the variation from lot to lot of components)
- ❑ **General guidelines** for radiation testing for ATLAS specify that 10 units be tested with actual load³.
- ❑ An **active measurement** of the response of the Bricks and components under irradiation was desired, thus a reasonable time period to search for any detrimental effects was chosen to be 30 minutes

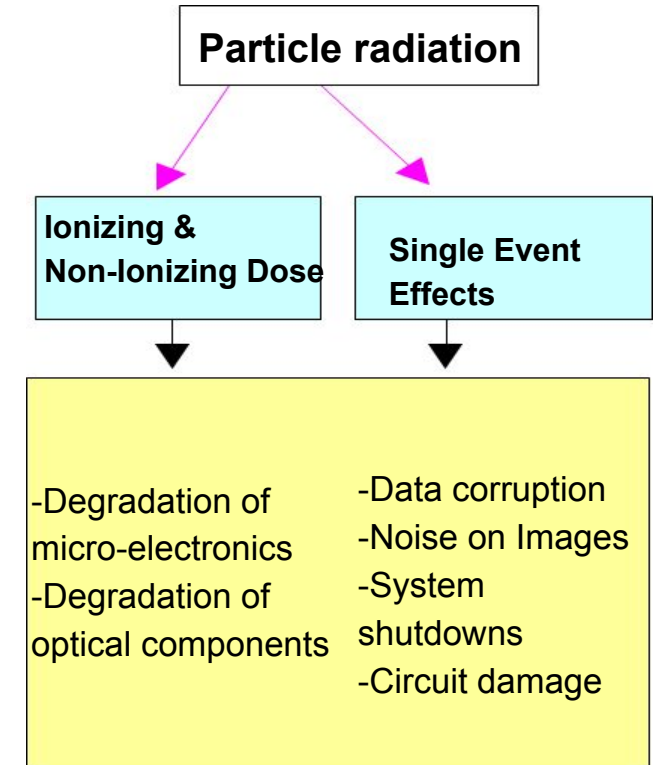
| Radiation Type | Location | Simulated Dose/ Fluence | SF_{sim} | SF_{lot} | Target Dose/ Fluence |
|--------------------------|----------|-------------------------|------------|------------|-----------------------|
| TID [Gy] | Barrel | 53.6 | 1.5 | 5 | (321) |
| | End-caps | 34.3 | 1.5 | 5 | (206) |
| SEE [p/cm ²] | Barrel | 5.3×10^{11} | 1.5 | 2 | 4.24×10^{12} |
| | End-caps | 9.8×10^{10} | 1.5 | 2 | 7.84×10^{11} |

3. ATLAS Radiation Policy:

<https://inspirehep.net/literature/1195265>

Radiation Testing: Component-Level tests

- ❑ **Component-level tests** of single batch to find candidates with
 - ❑ No/acceptable degradation with Total Ionizing Dose (TID) & Neutron Ionizing event loss (NIEL)
 - ❑ As well as no catastrophic failures due to Single Event Effects (SEE)
- ❑ **Challenges**
 - ❑ Huge number of (active) components to test and additional requirements i.e single lot components
 - ❑ Large variations in test conditions vs operating conditions
 - ❑ Availability of test facilities used for radiation testing of bricks: proton beams, gamma irradiation



- ❑ **Radiation testing** for SEE/TID performed (***Focus of presentation***) at Proton Irradiation Facility, PSI, Switzerland



Radiation testing is time and resource intensive,

Try optimize and reuse already tested components from older designs

Radiation Testing: Component-Level tests

There are two types of SEEs: non-destructive and destructive:

- ❑ Non-destructive, or soft, SEEs can be recovered by a system reset, re-programming/re-configuring the device or reprocessing of affected data.
- ❑ When a device fails, destructive or hard SEEs occur, resulting in lasting device or system damage.

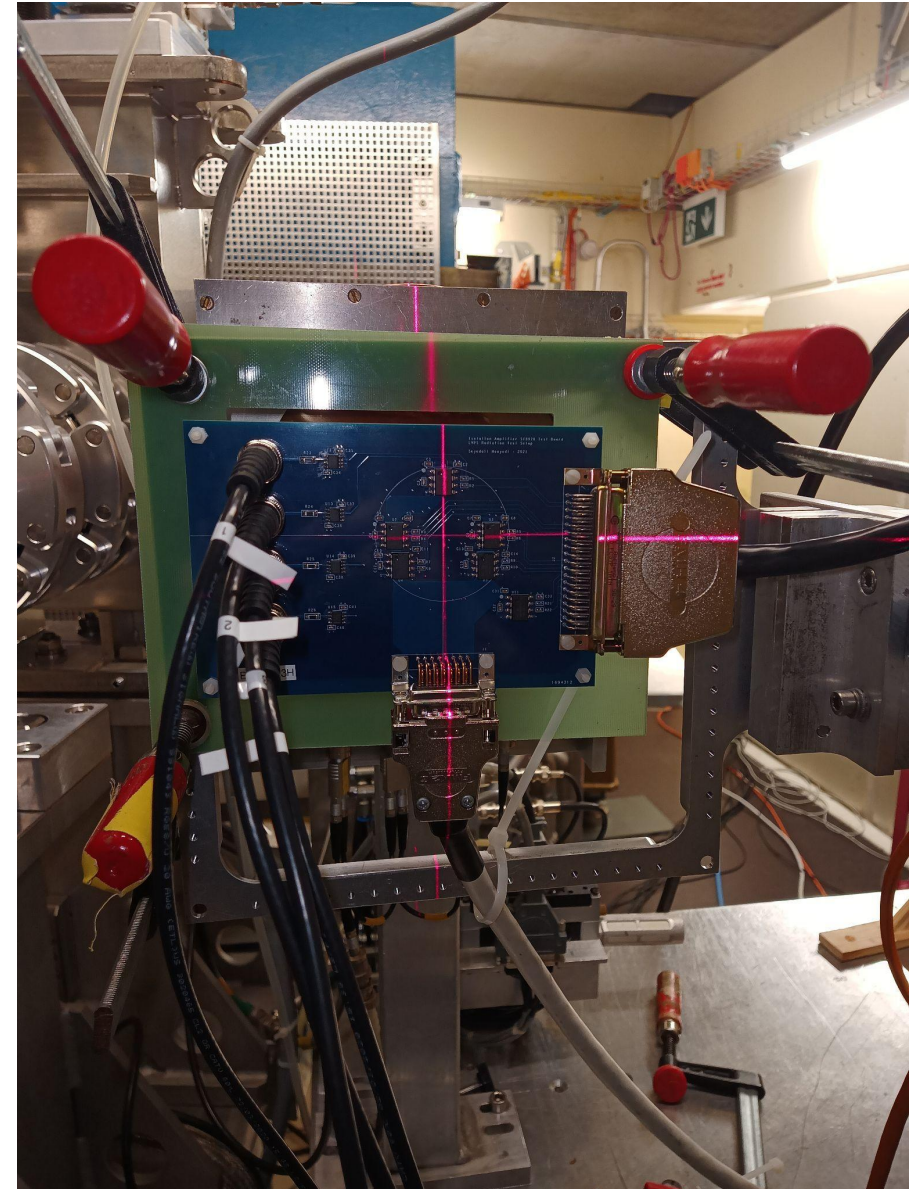
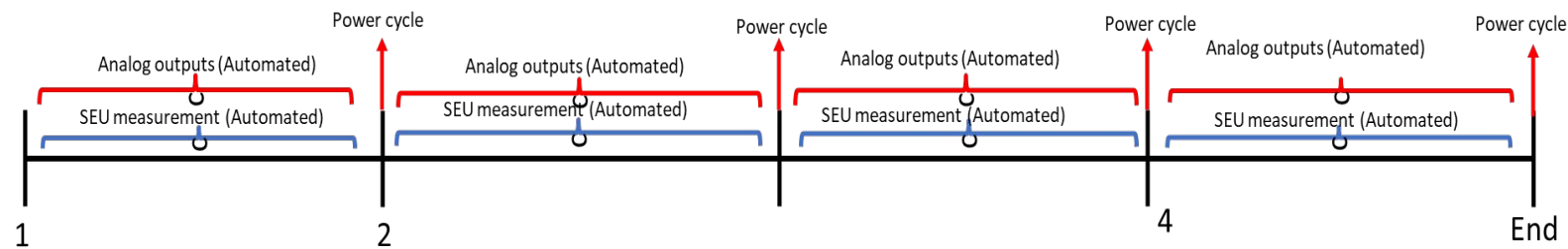
The components that were tested:

- ❑ **IR2110** MOSFET driver (10 pieces radiated + 1 reference piece all from the same batch)
- ❑ **SIHFS9N60A** MOSFET (16 pieces radiated + 4 reference pieces all from the same batch)
- ❑ **SI8920BC-IP** isolation amplifier (30 pieces radiated + 3 reference pieces from 3 batches) - *First results on presentation*

| Component | Part number | Required dose (Gy) | Board tested |
|---------------------|----------------|--------------------|--------------|
| Power MOSFET | SIHFS9N60A-GE3 | 200 | 2 |
| MOSFET driver | IR2110 | 200 | 1 |
| Isolation amplifier | SI8920 | 400 | 3 |

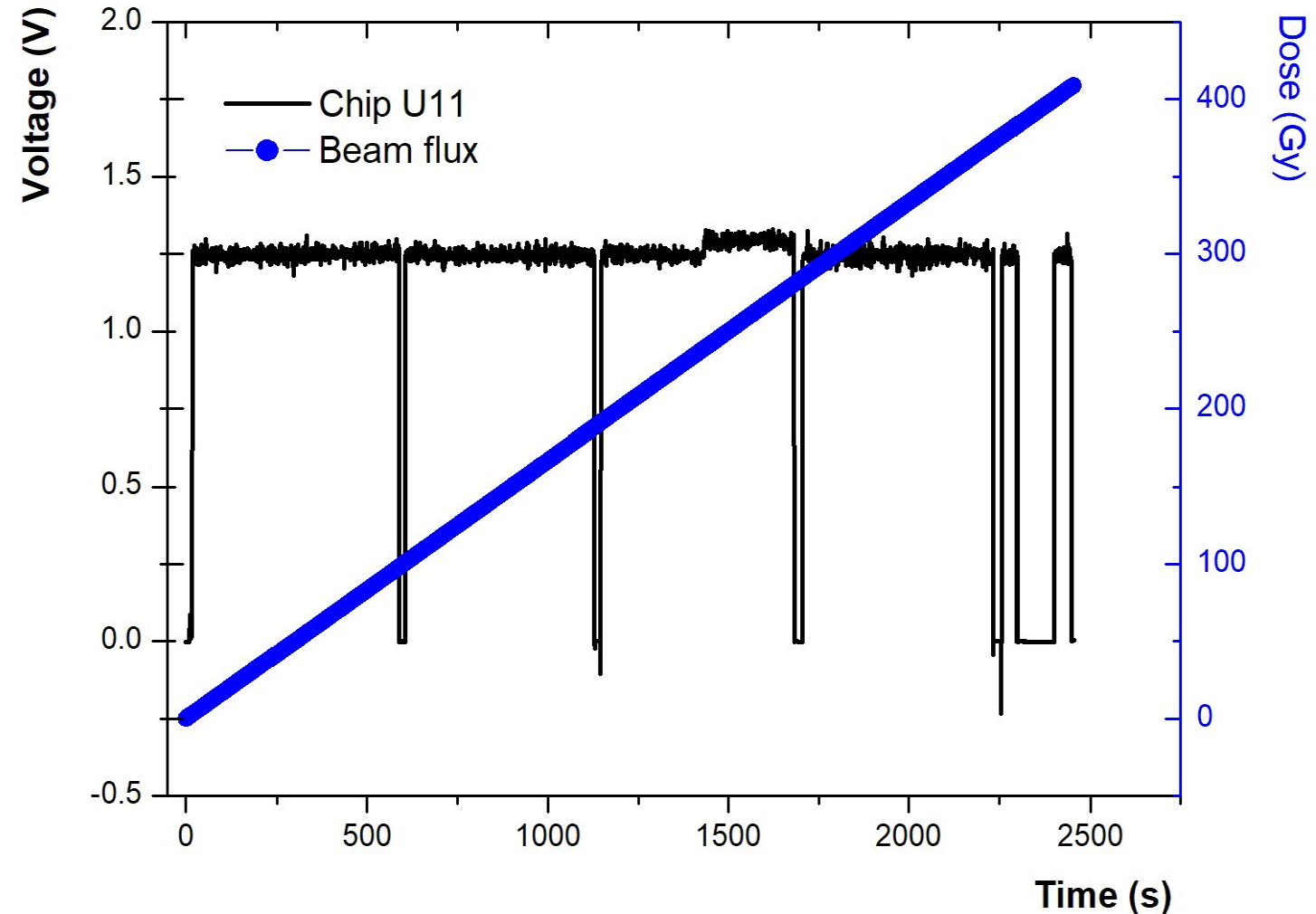
Experimental set-up: Component-Level tests

- ❑ The tests were performed with **200 MeV** proton beam with a flux of $3.5 \times 10^8 \text{ p/cm}^2/\text{s}$
- ❑ Each board was tested for around 30 minutes to reach $6.47 \times 10^{11} \text{ p/cm}^2$ (equivalent to 400 Gy)
- ❑ The chip has a fixed gain of 8.1, and by setting an input voltage of 0.15 V on all the chips, we expected to have an output voltage of 1.22 V
- ❑ All the 11 output voltages were being read by DAQ, and the output voltages of two of the chips (Chip #2 and Chip #10) were connected to a scope to see possible SETs.
- ❑ The result will only focus on the SI8920 Isolation amplifier



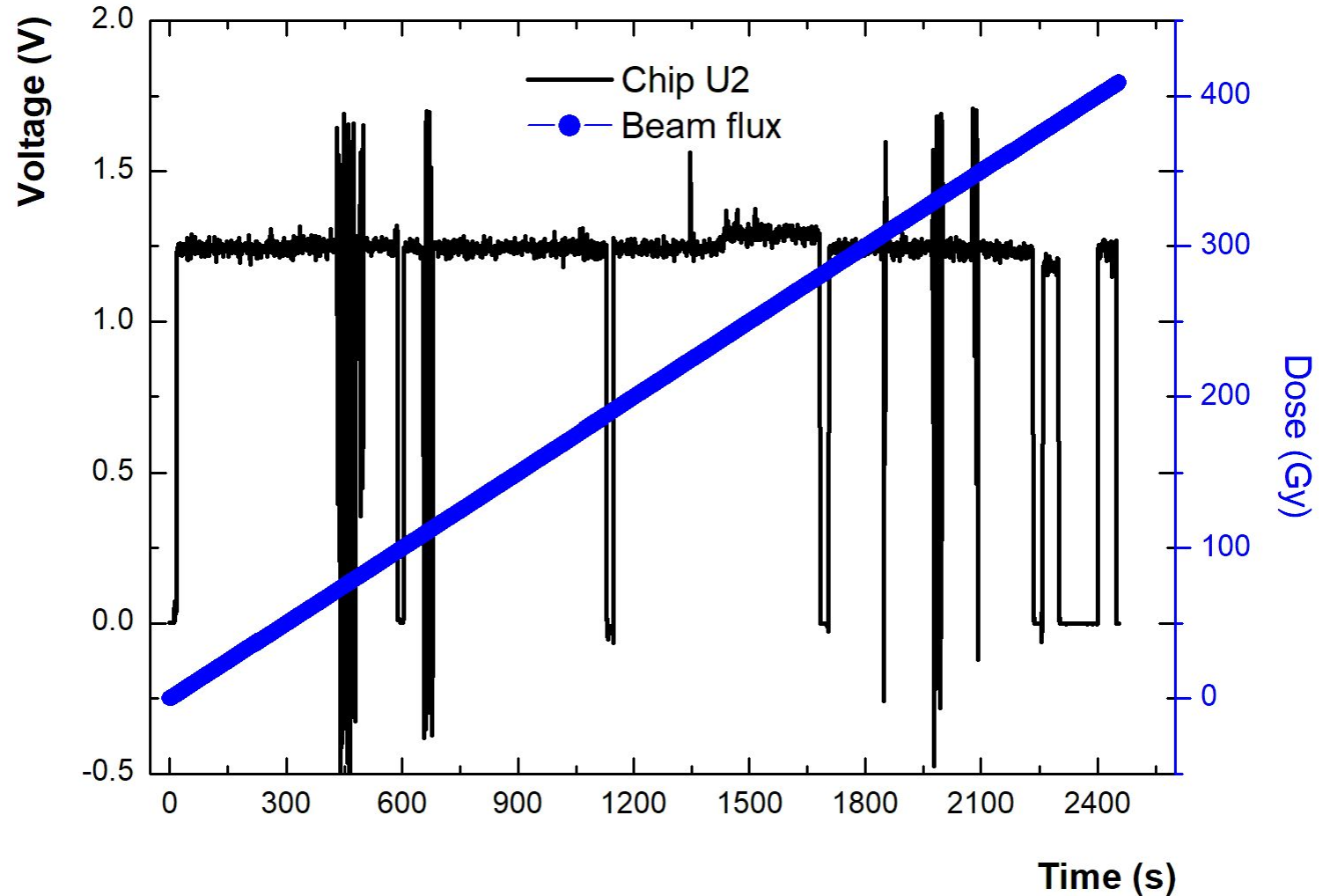
Latest Results: Component-Level tests

- ❑ The tests were performed in 4 runs, and there were a power cycle between each two consecutive runs
- ❑ There were also two power cycles at the end of the tests, just to see if any of the faulty chips will behave correctly after power cycle, or if any working chip will continue to work
- ❑ The results from the reference chip (chip #11) shows that this chip behaved completely normal during the test



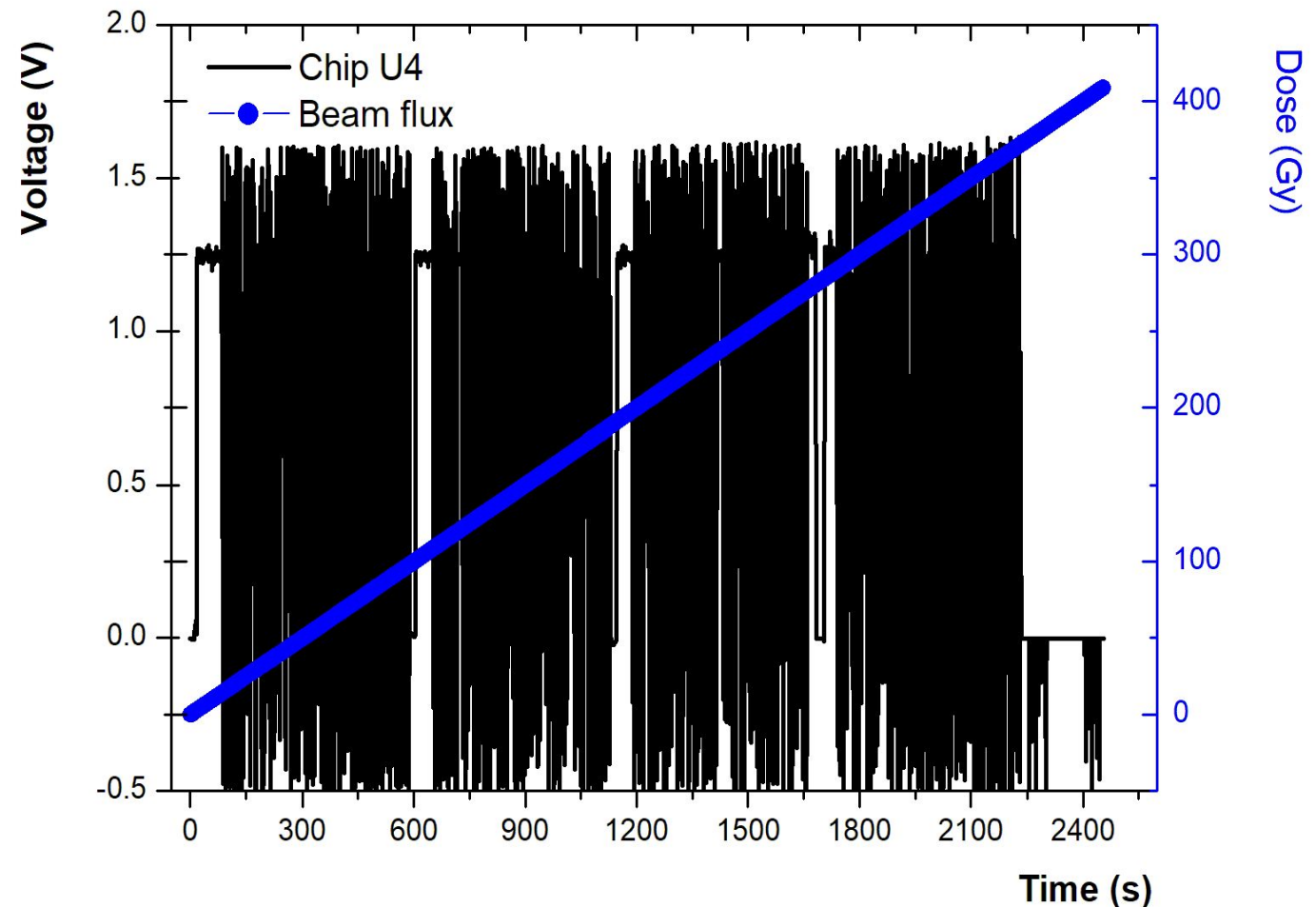
Latest Results: Component-Level tests

- ❑ The results from Chip #2 show that this chip almost behaved like the reference chip during the whole test, except for some time during the first, second and fourth runs, where it showed some fluctuations
- ❑ The fluctuations from Chip #2 went away without a need to power cycle
- ❑ The chip also survived the test after receiving 400 Gy



Latest Results: Component-Level tests

- ❑ The results from Chip #4 show that in all of the 5 runs, it goes to an unstable mode, where the output voltage fluctuates a lot
- ❑ The fluctuations started almost at the beginning of each run
- ❑ The fluctuations did not stop when the beam was stopped at the end of each run (a power cycle was needed)
- ❑ After the last run (receiving 400 Gy), the chip stopped working properly (due to TID effects), and even the two power cycles did not fix the issue



Latest Results: Component-Level tests

The MOSFETs were tested for SEEs by connecting the gate to source, and looking for transients on the drain

- ❑ No SEEs were observed
- ❑ The chips still has to be tested for characterization after they are back from PSI

The MOSFET drivers were tested for SEEs and for any possible drift in pulse shapes

- ❑ No SEEs or possible drifts were observed. They will be tested again after arriving at CERN
- ❑ Preliminary results for these two chips are very satisfactory



| Component | Part number | Required dose (Gy) | SEE observed |
|---------------------|----------------|--------------------|-------------------------|
| Power MOSFET | SIHFS9N60A-GE3 | 200 | No |
| MOSFET driver | IR2110 | 200 | No |
| Isolation amplifier | SI8920 | 400 | Yes (4 out of 10 Chips) |

ICPP LVPS SA team



Roger Van Rensburg

Front row from left to right: Bruce Mellado, Jacques Klopper, Charles Sandrock, Thabo Lepota, Nkosiphendule Njara, Edward Nkadimeng, Ryan Mckenzie.