INSTITUTE FOR COLLIDER PARTICLE PHYSICS

UNIVERSITY OF THE WITWATERSRAND

Quality assurance testing of the ATLAS Tile-Calorimeter Phase-II upgrade low-voltage power supplies

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Talk Outline

- The ATLAS Tile-calorimeter
- TileCal Phase II Upgrade
- Low-Voltage Power Supply Brick
- Quality Assurance testing
- Initial Testing
- The Initial Test Station
- Burn-in Testing
- The Burn-in Test Station
- Conclusion

The ATLAS Tile-Calorimeter

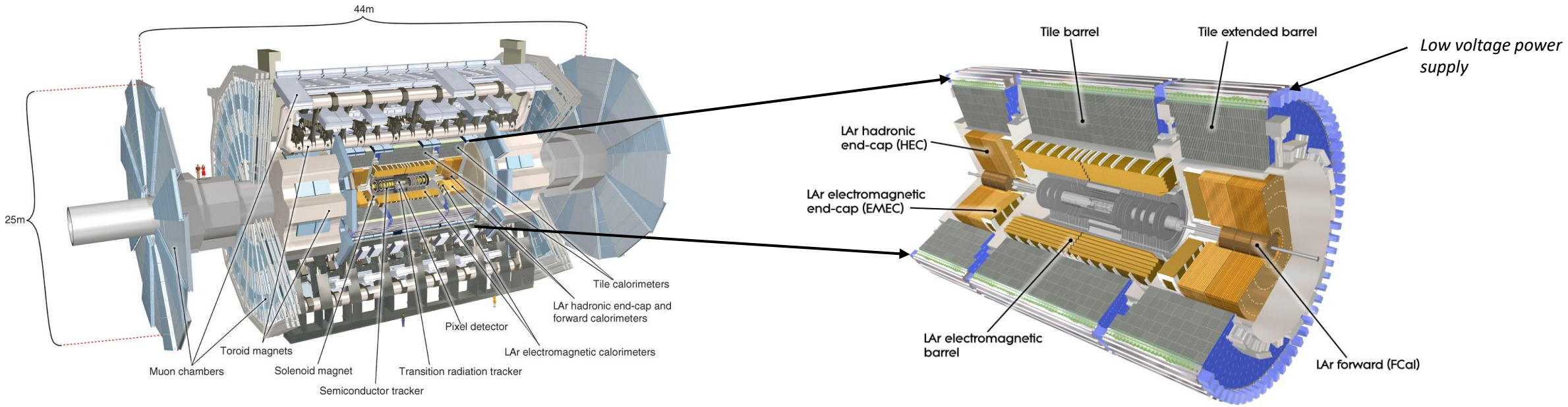
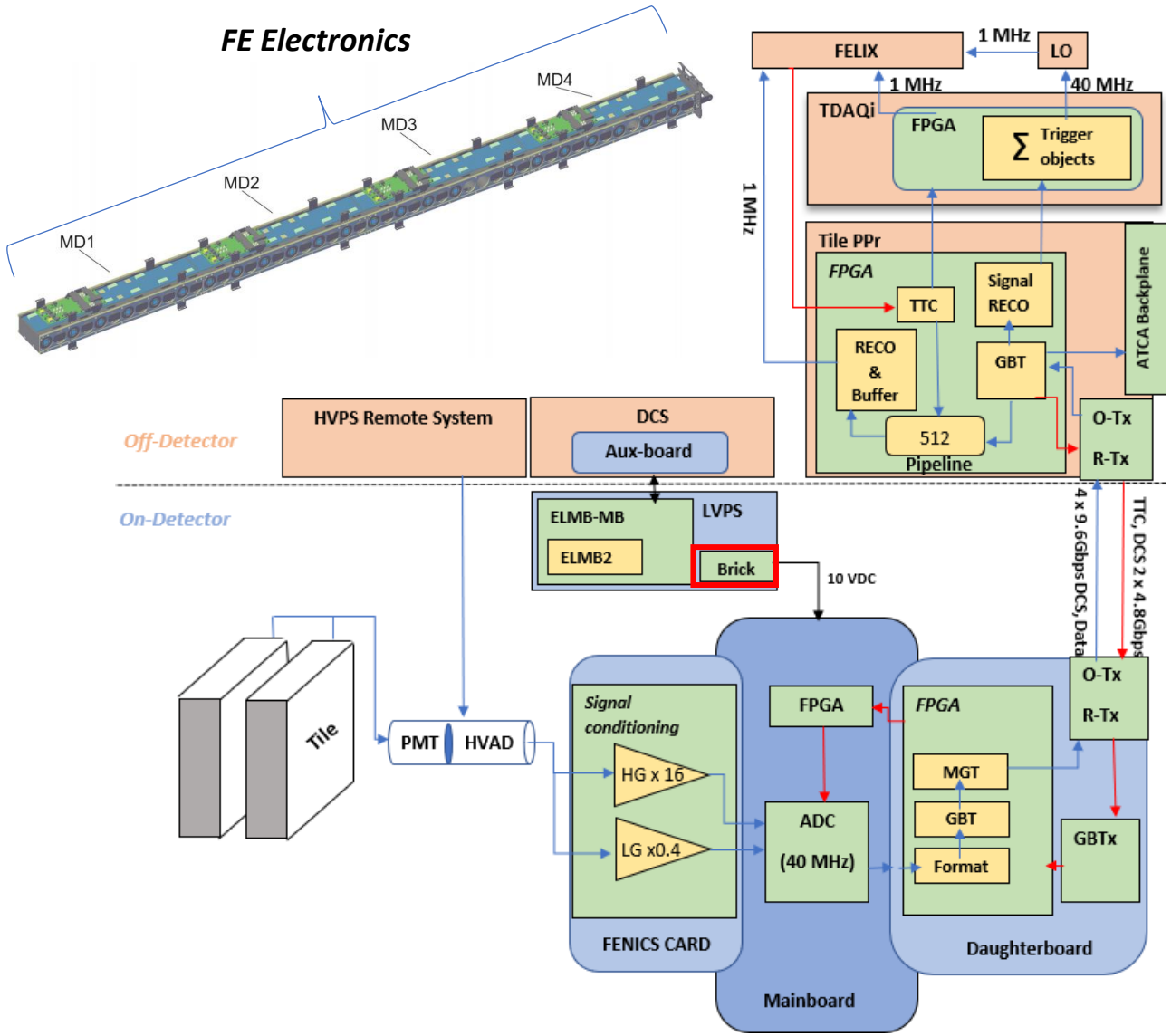


Fig. Left - The ATLAS detector, Right - The ATLAS inner Barrel, Right

- The Tile Calorimeter (TileCal) is a sampling calorimeter which forms the central section of the Hadronic calorimeter of the ATLAS experiment.
- TileCal performs several critical functions within ATLAS such as: the measurement and reconstruction of hadrons, jets, hadronic decays of τ-leptons and missing transverse energy. It also participates in muon identification and provides inputs to the Level 1 calorimeter trigger system.
- The detector is located within the region $\eta < |1.7|$ and is partitioned into four barrel regions. Each barrel region consists of 64 wedge shaped modules which cover $\Delta\varphi \sim 0.1$ and are composed of plastic scintillator tiles, functioning as the active media, inter-spaced by steel absorber plates.

TileCal Phase II Upgrade

- **New readout, Front-end and Back-end electronics** - to stream data to trigger processor at 40 MHz crossing rate providing fully digital data to the trigger processors;
- **Improved radiation hardness** of electronics for high luminosity environment.
- **New mechanical frames** to house the front-end electronics;
- **HV**(PMT) will be controlled remotely;
- **LV**: Unified Input to FE electronics power to 10V; individual Brick control
- **Upgraded calibration systems**(Cesium and Laser);
- **Redundancy introduced in data links**;
- **Replacement of 10% of PMTs** associated with the most exposed cells;



MD: Mini Drawer
SD: Super Drawer
PMT: Photo multiplier Tube
FELIX: Front-End Link eXchange
TDAQi: Trigger and Data Acquisition Interface
FPGA: Field Programmable Gate Array
PPr: Pre Processor
ADC: Analog To Digital Converter
HVAD: High Voltage Active Divider
DCS: Detector Control System
ELMB: Embedded Local Monitoring Board
ELMB-MB: Embedded Local Monitoring Board Mother Board
HV: High Voltage
LV: Low Voltage
FE: Front-End

Low Voltage Power Supply Brick

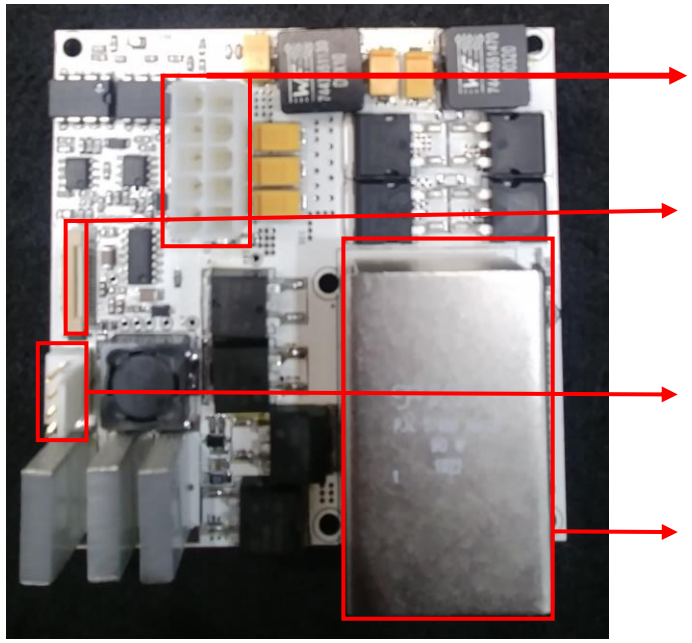


Fig. *South African High efficiency LVPS Brick top view .*

- A transformer coupled buck converter.
- Converts bulk 200VDC power to the 10VDC which is then distributed to the Front-end electronics.
- Makes use of inbuilt protection circuitry – Over voltage protection, Over current protection and Over temperature protection.
- 1136 LVPS Bricks to be locally produced by SA-CERN over the next two years.
- The required lifetime of a Brick within TileCal is ~ 20 years.

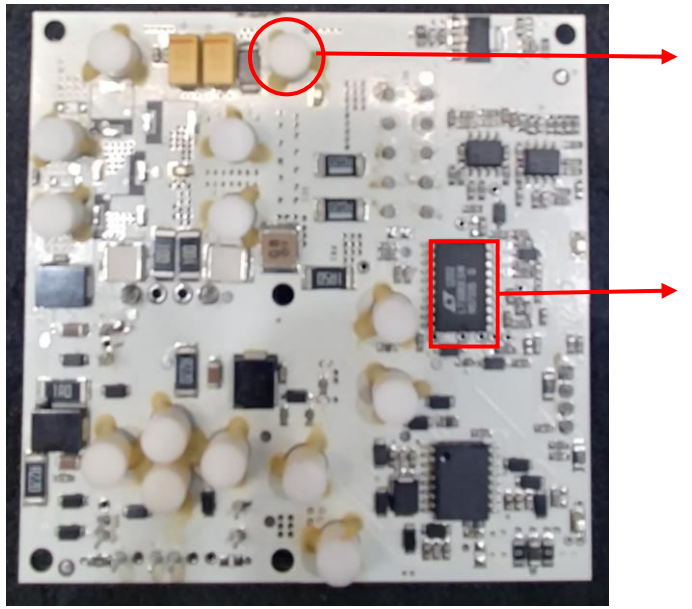


Fig. *South African High efficiency LVPS Brick bottom view .*

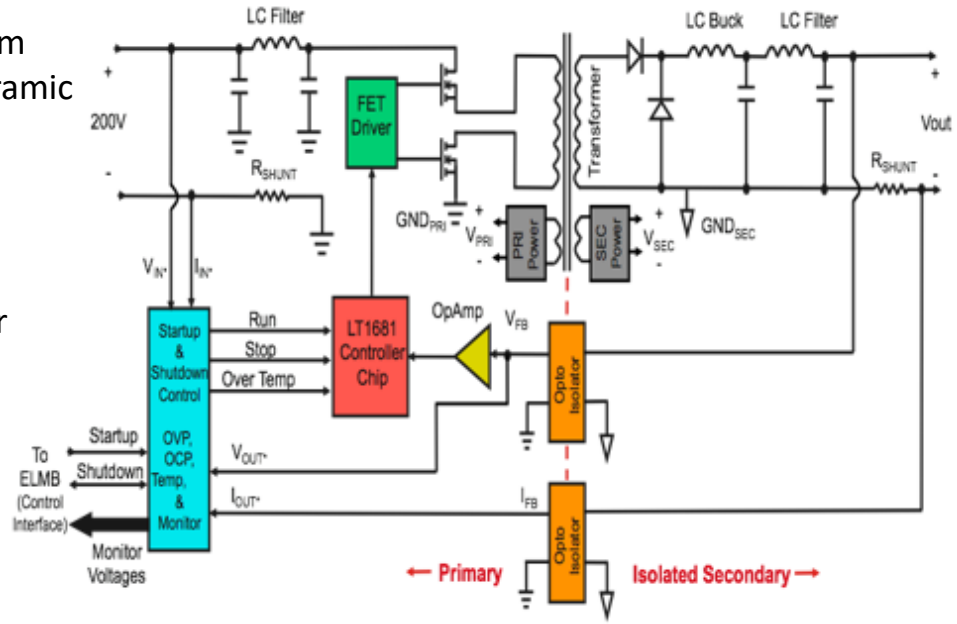


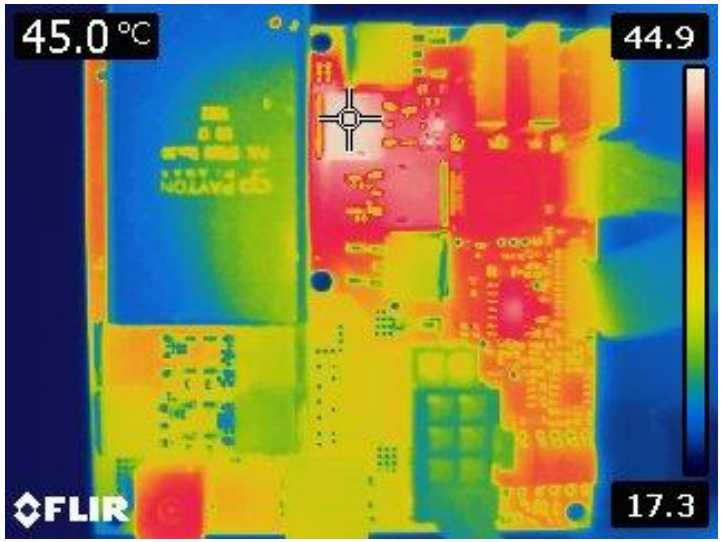
Fig. *LVPS Brick functional block diagram.*

Locally produced elements:

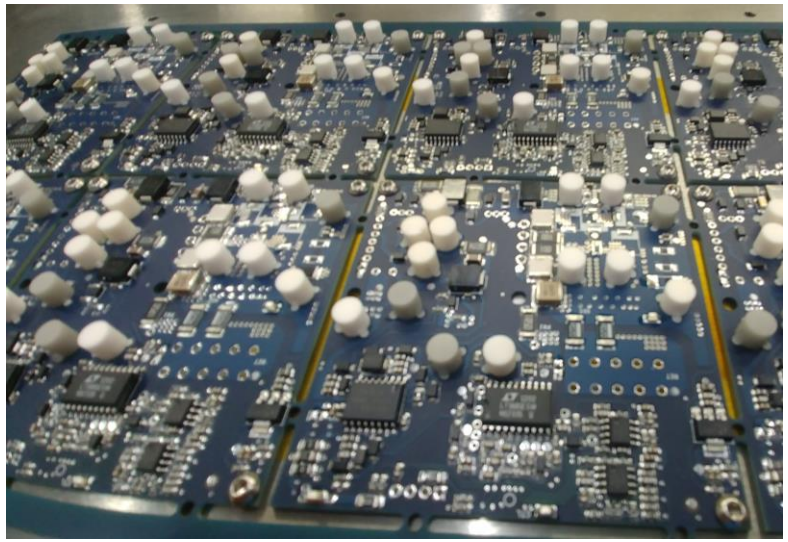
- ✓ Printed circuit boards
- ✓ Ceramic posts
- ✓ Production of final product

Low Voltage Power Supply Brick

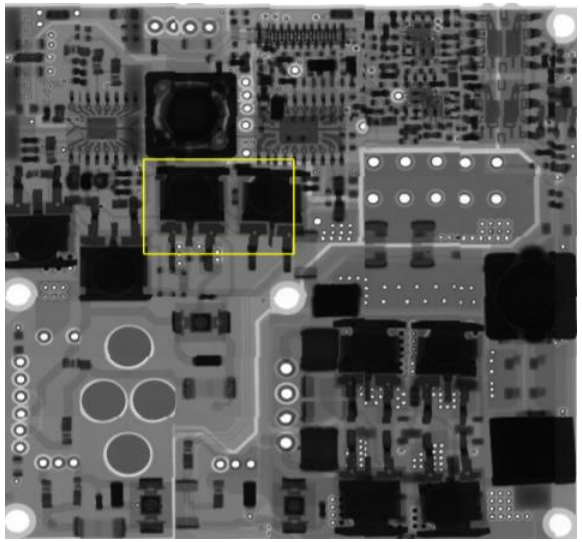
Thermography



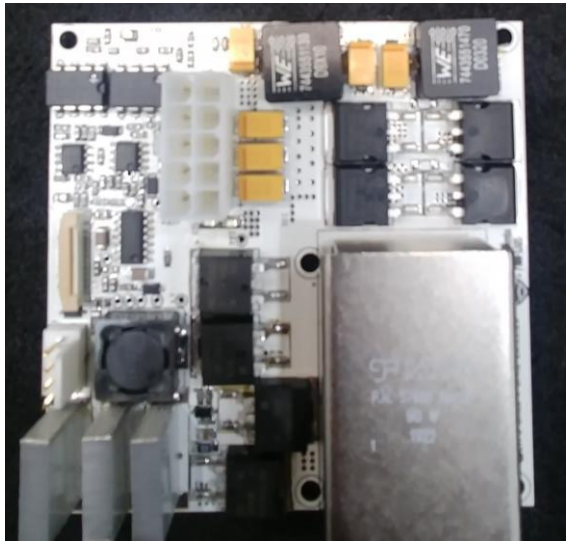
Production



X-ray scans

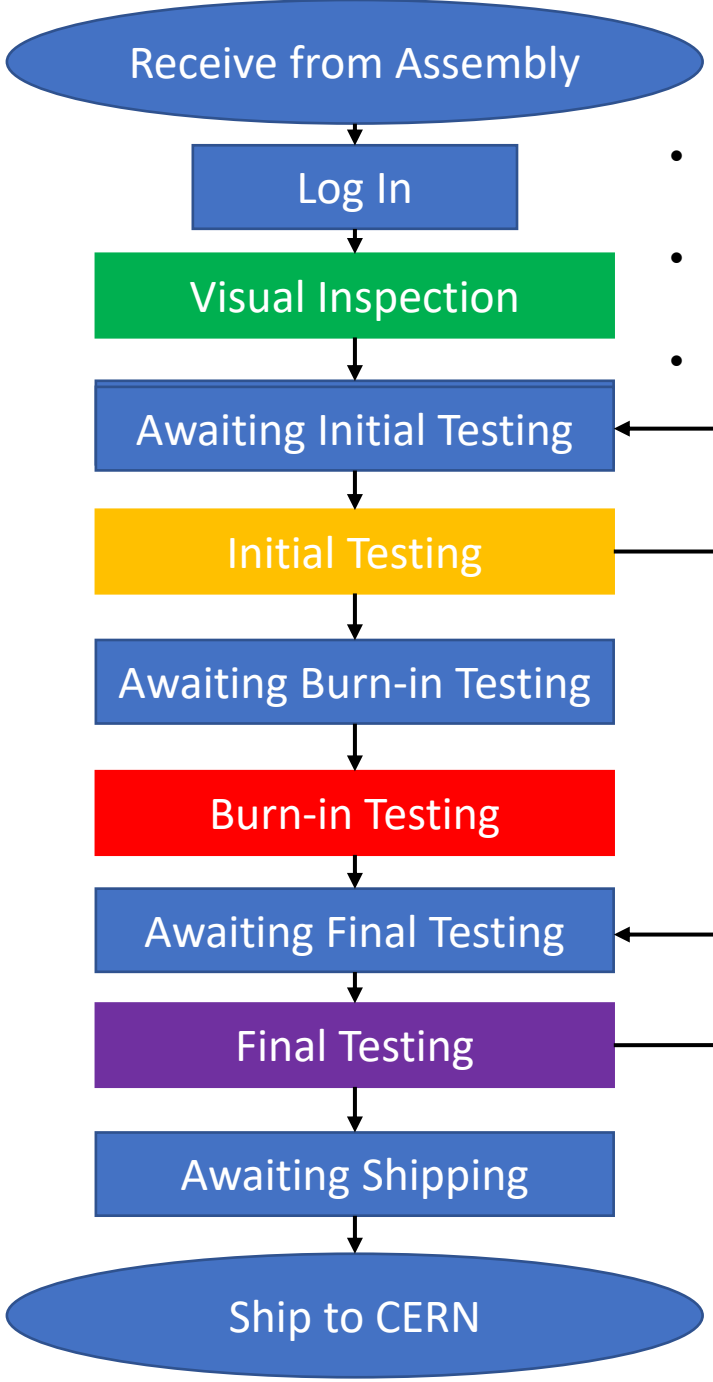


High efficiency
LVPS Brick



Quality Assurance Testing

- Due to the Bricks being located within the Inner-barrel of ATLAS access to them is on the order of once per year. Therefore, any failures will persist for up to a year.
- Reliability of the Bricks is a key concern and as such a rigorous quality assurance procedure is to be implemented.
- The procedure consists of a visual inspection, Initial testing, Burn-in testing and Final testing.



Initial testing: Verifies performance metrics of Bricks once received from manufacturer.

Burn-in testing: Performs accelerated aging of the electronic components of a Brick.

Final testing: Verifies performance metrics of Bricks once more to ensure that Burn-in testing did not cause any damage to the Bricks.

Initial Test Station

The Test station is composed of 3 key elements:

1. Mechanics – Test fixture
2. Electronics – Oscilloscope, HV power supply, LV power supply, Electronic load, DAQ card and a custom Interface board.
3. Software – Custom LabVIEW control program (Please see Edward Nkadimengs poster)

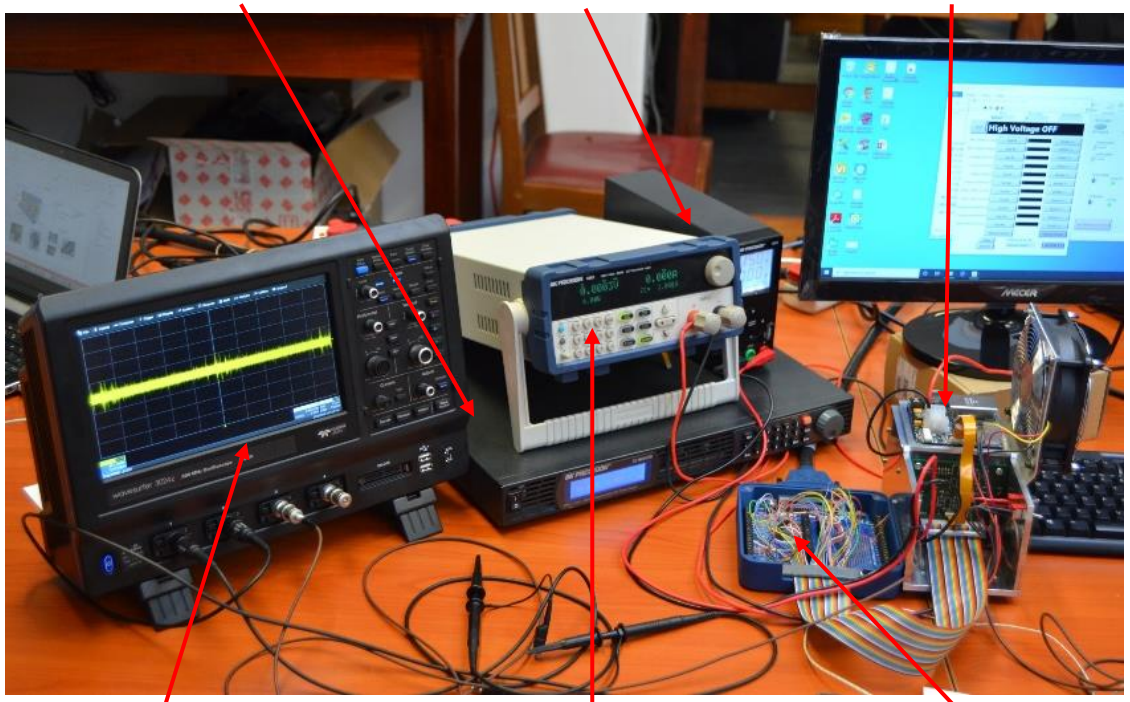


Fig. *Wits Initial Test Station.*

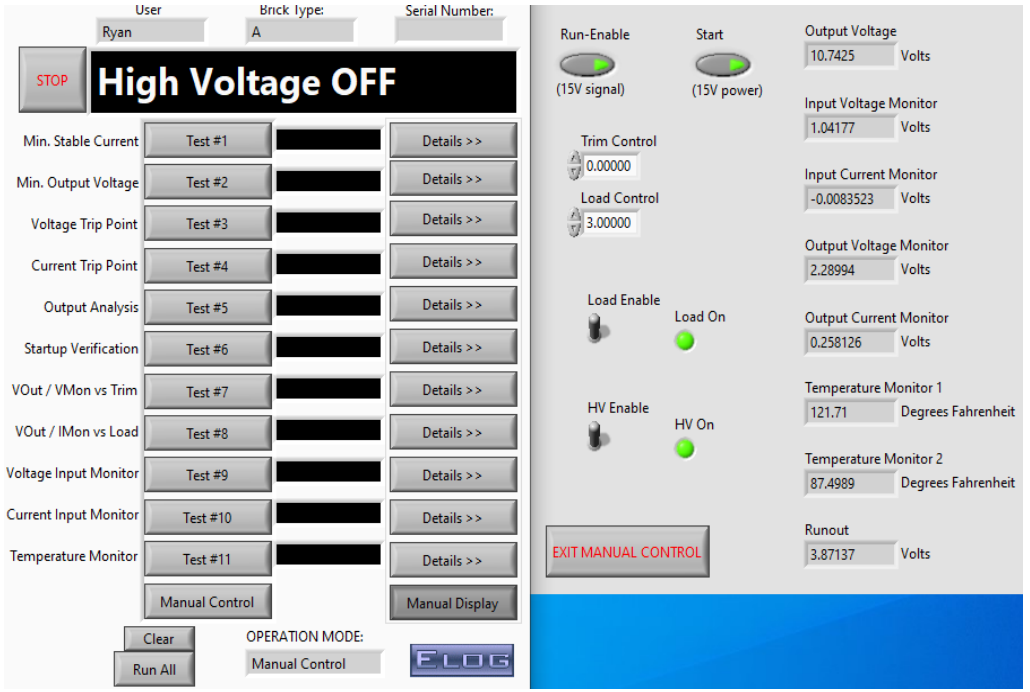


Fig. *Wits Initial test station LabVIEW control program*

Fig. *Wits Initial Test Station fixture.*

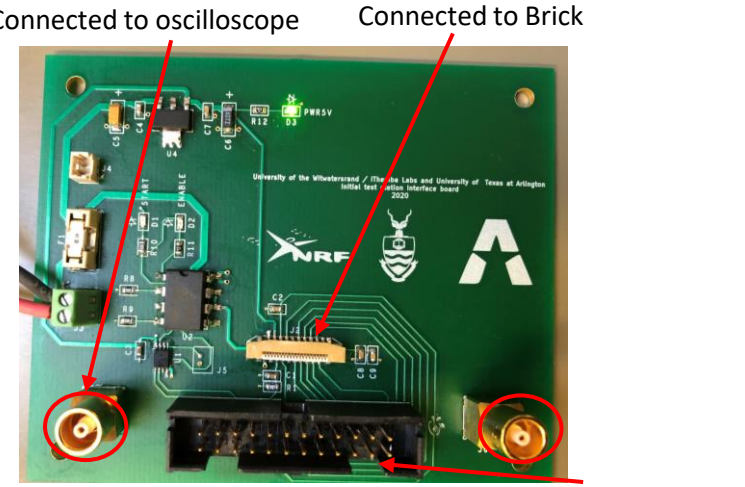


Fig. *Wits Initial Test Station interface board.*

Initial Testing of an LVPS Brick

Parameter	Minimum	Maximum
Frequency Standard Deviation	0	1000
Duty Cycle Standard Deviation	0	0.1
Frequency Max (Hz)	290000	350000
Frequency Min (Hz)	250000	310000
Minimum Stable Load (A)	2	2.1
Minimum Output Voltage (V)	9.8	10.2
Over Voltage Protection (V)	11.5	12
Over current Protection (A)	10.25	10.75
Output Root Mean Square Voltage	0	0.5
Clock duty cycle average	0	40
Clock Duty Cycle Standard Deviation	0	0.15
Start-up delay (Max) (s)	0.08	0.2

Fig. *Wits Initial Test Station performance metrics.*

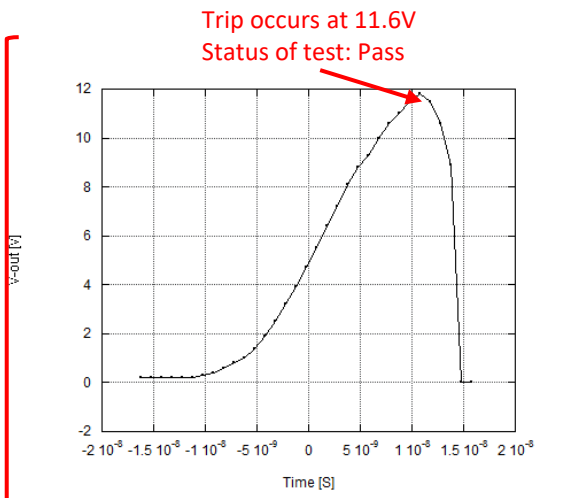


Fig. *LVPS Brick over voltage protection test illustrating a pass.*

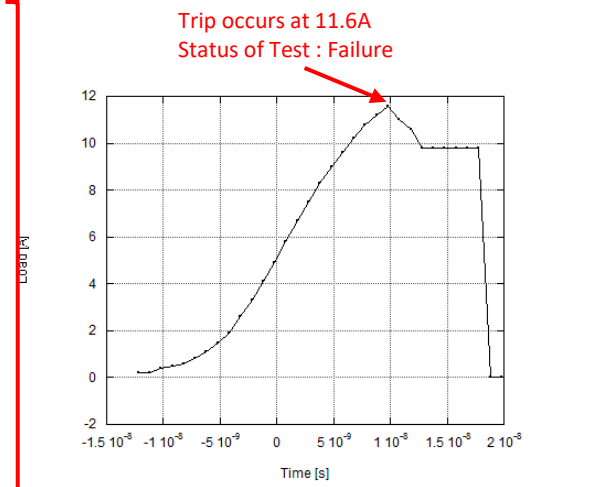


Fig. *LVPS Brick over current protection test illustrating a failure.*

A look at Test 5: Output analysis

- Test 5 serves as an analysis of the outputs of a LVPS brick. This test ensures that the bricks out characteristics are within the range that the TileCal Front-end electronics can accept.
- The brick is operated at nominal load (2.5 A). – This is to be amended to 2.3 A
- The Bricks monitoring hardware registers the performance
- Observe that all but one of the sub-tests yielded a desirable result.

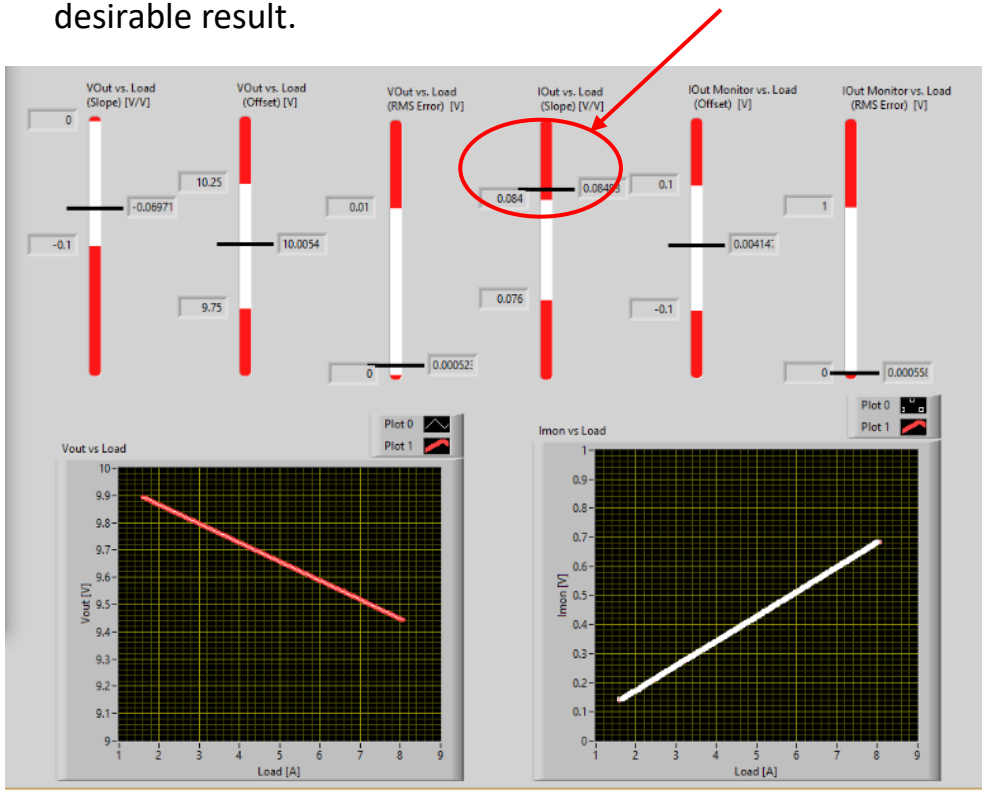


Fig. *Test 5 output analysis*

Burn-in Testing

τ_o = Equivalent operating time at T_o
τ_s = Stressed lifetime
T_o = $Operating\ temperature$
T_S = $Stress\ temperature$
E_a = $Activation\ energy$
k = Boltzmanns constant
AF_T = $Temperature\ acceleration\ factor$

- A form of accelerated aging of electronic components.
- Improves LVPS Brick reliability once on detector by encouraging failures associated with the infant mortality region before installation.
- The operation of the LVPS bricks at a higher load and operating temperature should cause the components to fail immediately within the Burn-in station as opposed to prematurely within ATLAS.
- We want to stimulate failure mechanisms which are experienced within normal operation.
- Primary components of concern are illustrated in the simplified signal flow diagram. It is assumed that any failure of the components shown will open the signal flow loop and cause a failure.

$$\frac{\tau_o}{\tau_s} = AF_T = \exp[\frac{E_a}{k}(\frac{1}{T_o} - \frac{1}{T_S})]$$

The Arrhenius equation

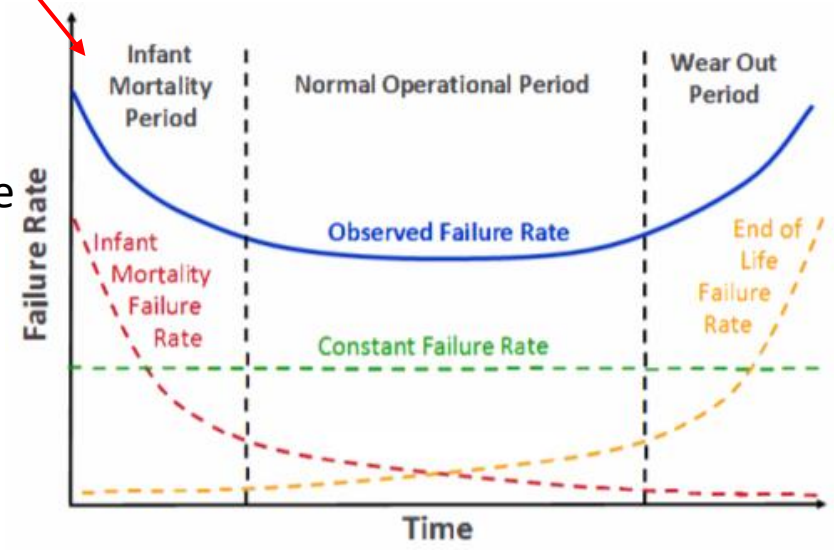


Fig. *Bathtub curve of electronics failure rate.*

Fig. *C29 KEMET capacitor failure rate calculator.*
https://ec.kemet.com/design-tools/fit-calculator/

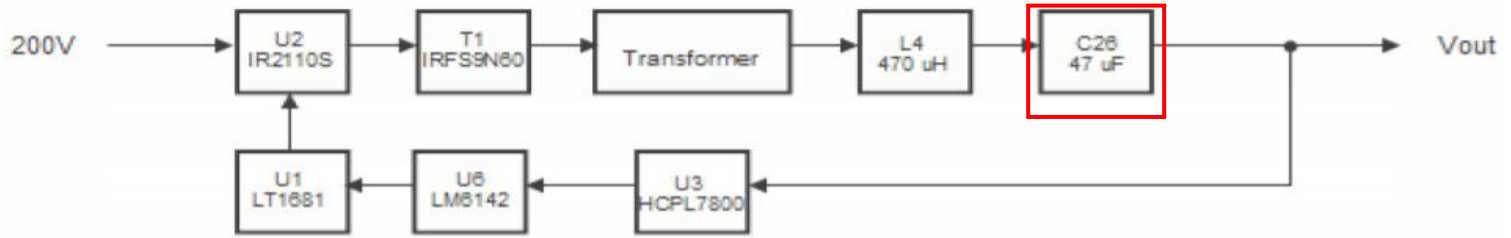


Fig. *LVPS Brick simplified signal flow diagram.*

Burn-in Test Station Overview

Burn-in procedure:

- Endurance run approx. 8hrs at 5A
- Operating temperature to be determined during calibration.
- 8 Bricks are undergo burn-in simultaneously.

The Test station is composed of 4 key elements which work together to facilitate the Burn-in of 8 Bricks per test cycle.

Mechanics – Required to contain the Burn-in station electronics, provide thermal and electrical insulation.

Cooling system – Provides active cooling of the Bricks as well as the Dummy-Load boards. Allows for the control of the Bricks operating temperature.

Electronics – Will be covered in detail the next slide.

Software – Allows for the control of the custom electronics, the HV power supply as well as the storage and real time viewing of data.

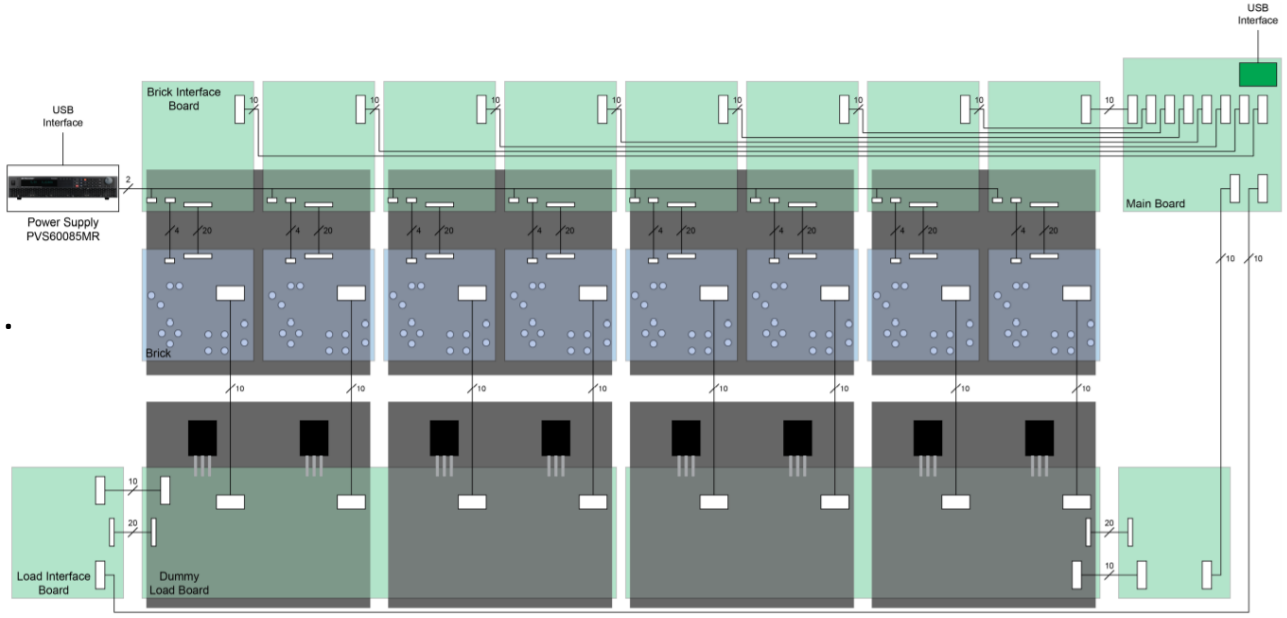


Fig. *Brick Burn-in station block diagram. Seyedali Moeyedi*

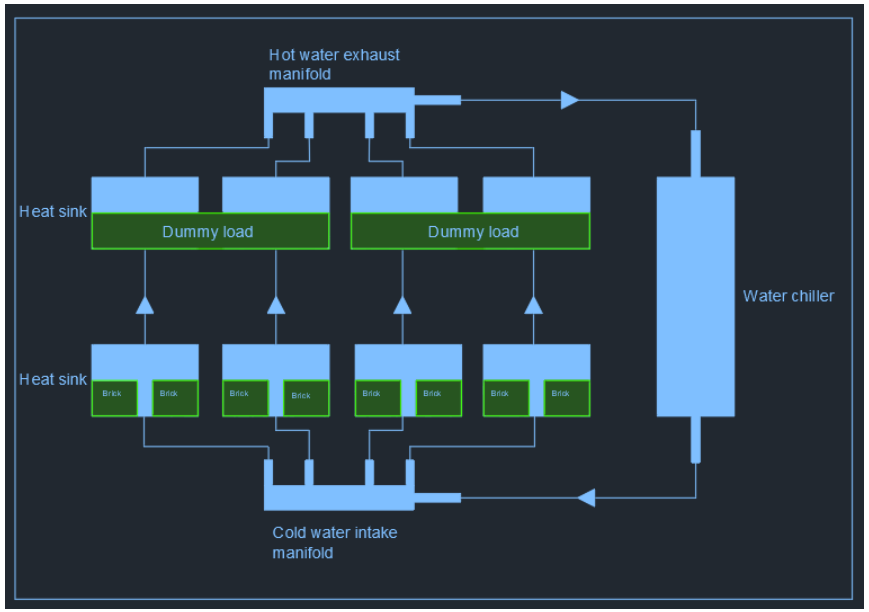
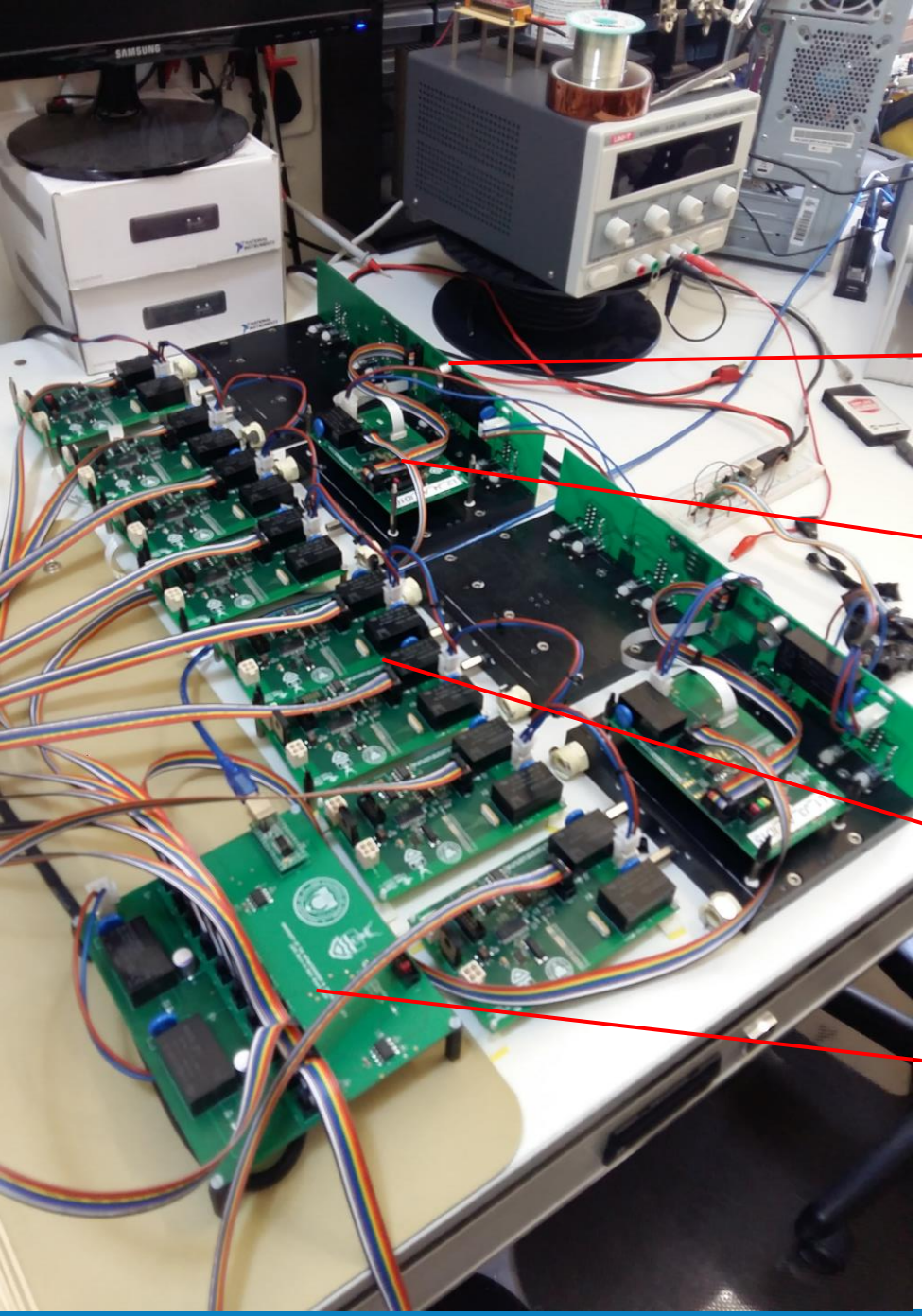


Fig. *Brick Burn-in station cooling system block diagram.*

Burn-in Test Station Electronics



Dummy-load board:

- Acts as a variable electronic load for the LVPS bricks.
- Converts power received into heat via MOSFETS.
- Heat dissipated via cooling plates.

Load Interface board:

- Interfacing between main board and Dummy-load board.
- Allows for the control of the load applied to the Bricks.

Brick Interface board:

- Interfacing between main board and an individual Brick.
- Used to control and monitor a Brick.
- Acts as a switch for the 200 VDC input to a Brick.

Main board:

- A multiplexer to each Interface board.
- Facilitates serial communication with PC.

Fig. *Testing of the WITS Burn-in station before final integration with the chassis and cooling system..*

Conclusions

TileCal & Phase II upgrade.

LVPS Brick Function and production.

Quality assurance testing.

Initial/Final testing & Burn-in testing.

What next?

- Completion and calibration of Burn-in station.
- Production of Bricks.
- Testing and Burn-in of Bricks.

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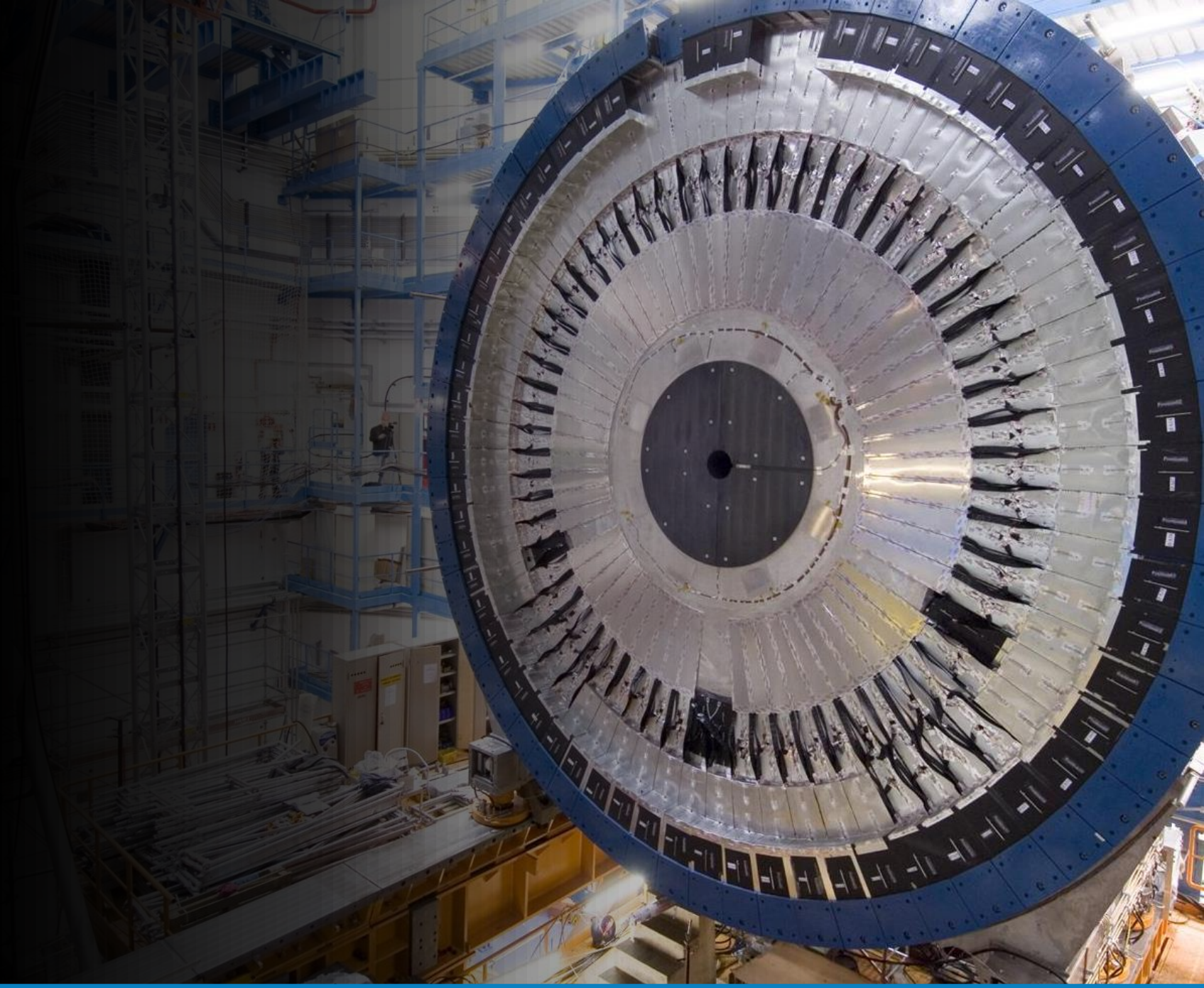
NRF National Research Foundation

Reference slides



TileCal Phase-II upgrade

- In the year 2027 the start of the operation of the High-luminosity Large Hadron Collider (HL-LHC) is planned with a foreseen peak luminosity of $5 \times 10^{34} cm^{-2} s^{-1}$.
- The resulting HL-LHC environment has necessitated the development of new electronics, both on and off detector, in order to ensure the continued peak performance of TileCal.

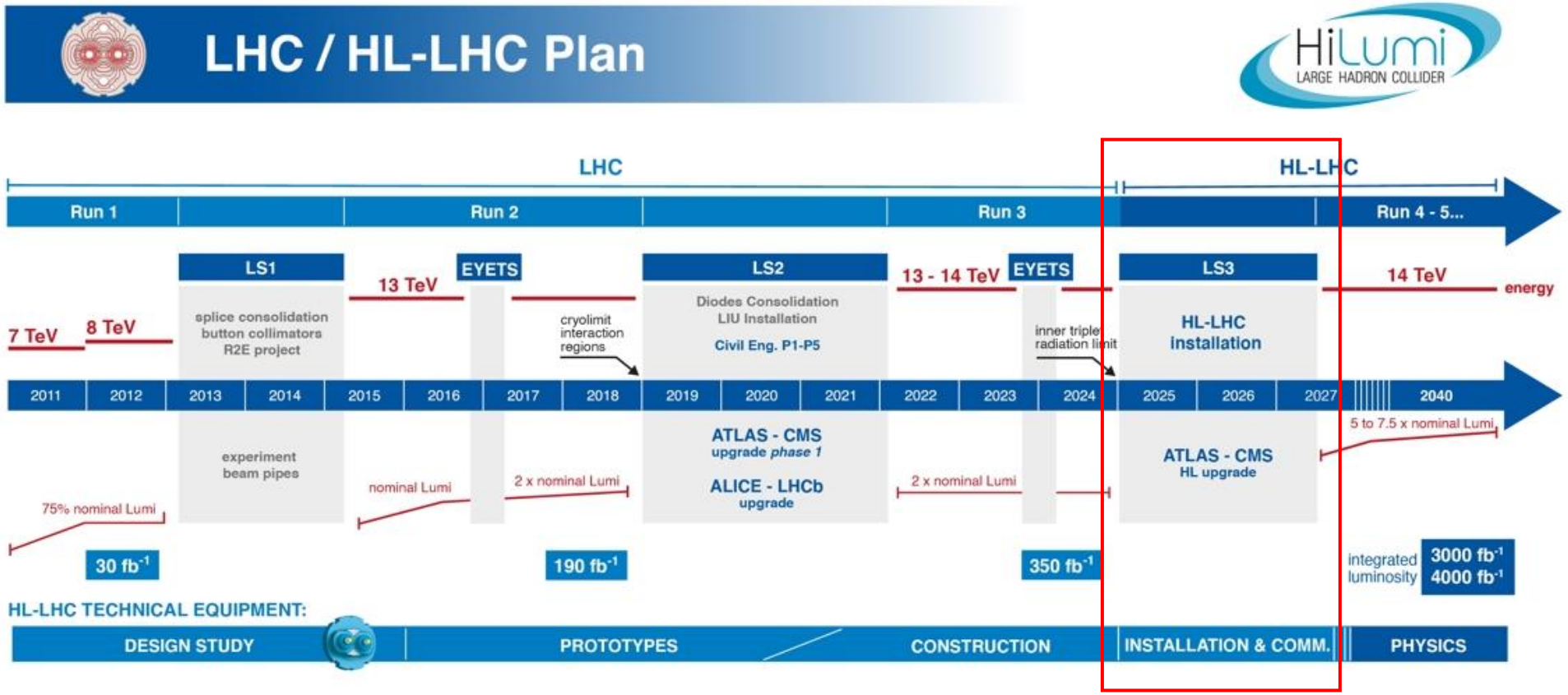


Fig. *LHC/ HL-LHC Plan (last update January 2021)* [The HL-LHC project | High Luminosity LHC Project (cern.ch)]

TileCal Phase-II Upgrade power distribution

High Voltage (HV) Distribution System

• The HV distribution system provides regulated high voltage to individual HVADs. It consists of HVremote boards that provide primary HV which is distributed to the HVADs via passive HVbus boards located within the Minidrawers.

• The upgrade removes the radiation hardness requirements of the HV regulators as regulation is now implemented off-detector

Low Voltage Distribution, Control and Monitoring System (LVDCMS)

• This system provides low voltage power to the front-end electronics of the Superdrawers. The off detector Auxiliary boards (AUXboards) operate as 200 VDC power supplies as well as perform control and monitoring functions via the Embedded Local Monitoring Board (ELMB) of the Low Voltage Power Supplies (LVPS), of which there is one per TileCal module. The new on detector LVPS is radiation hard and is comprised of eight Bricks which function to step-down the 200 VDC received from the AUX boards to the 10 VDC required by the Point-of-load regulators located on the MBs as well as an ELMB.

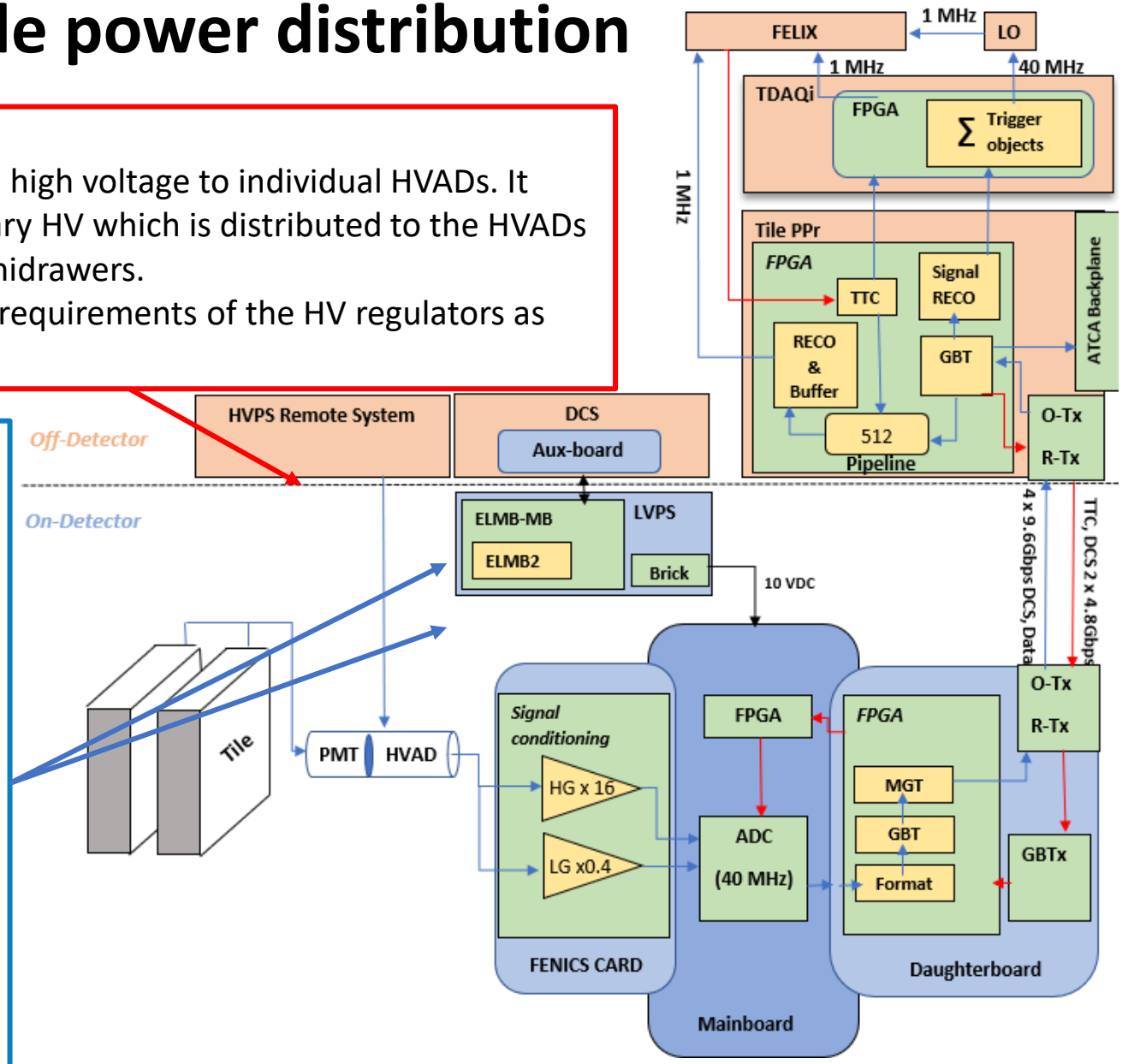


Fig. The upgraded readout chain and power distribution of TileCal.

MD: Mini Drawer
SD: Super Drawer
PMT: Photo multiplier Tube
FELIX: Front-End Link eXchange
TDAQi: Trigger and Data Acquisition Interface
FPGA: Field Programmable Gate Array
PPr: Pre Processor
ADC: Analog To Digital Converter
HVAD: High Voltage Active Divider
DCS: Detector Control System
ELMB: Embedded Local Monitoring Board
ELMB-MB: Embedded Local Monitoring Board Mother Board
HV: High Voltage
LV: Low Voltage
FR: Front End

TileCal Phase-II Upgrade mechanics

- The On-detector electronics are housed in a new modular configuration in which one drawer (Superdrawer) is composed of 4 functionally independent Minidrawers (MD).
- The new configuration simplifies installation and manipulation creating better conditions for servicing within the high radiation environment.

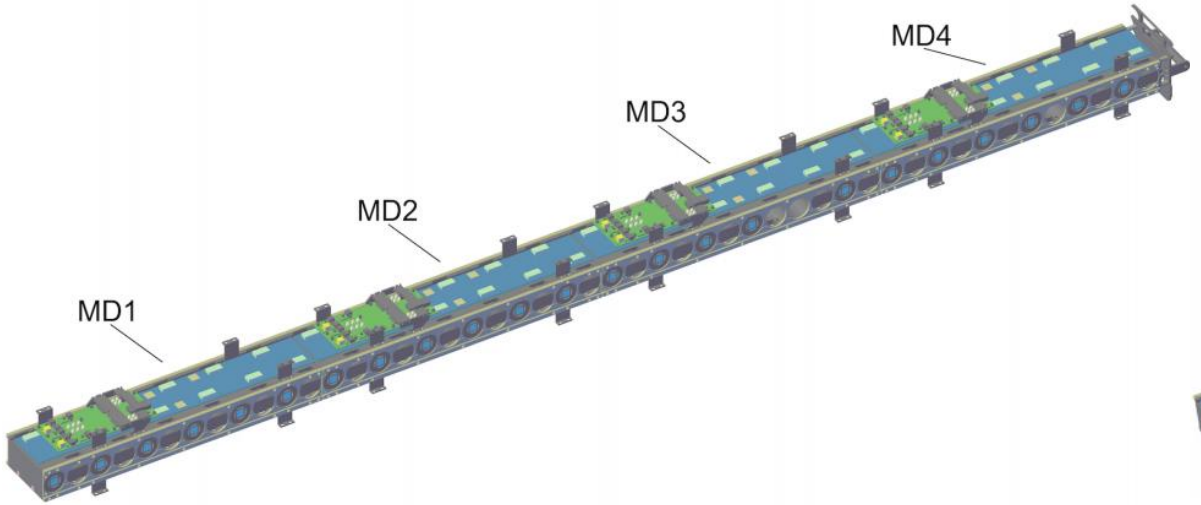


Fig. Tile new super-drawer architecture, ATL-TDR-028 · LHCC-2017-019, pg 69

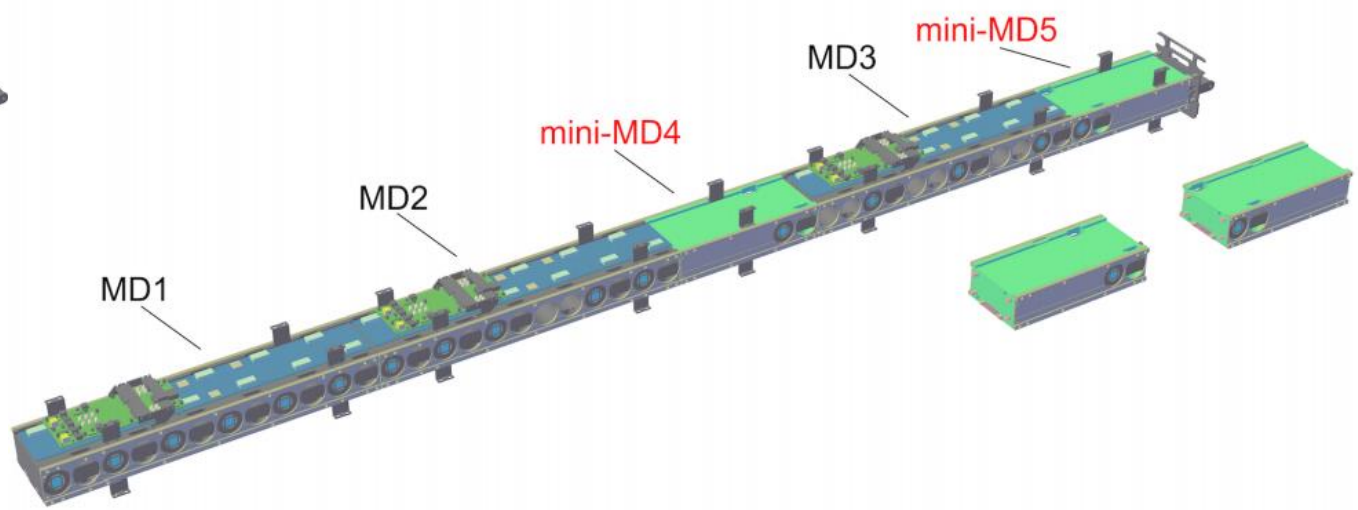
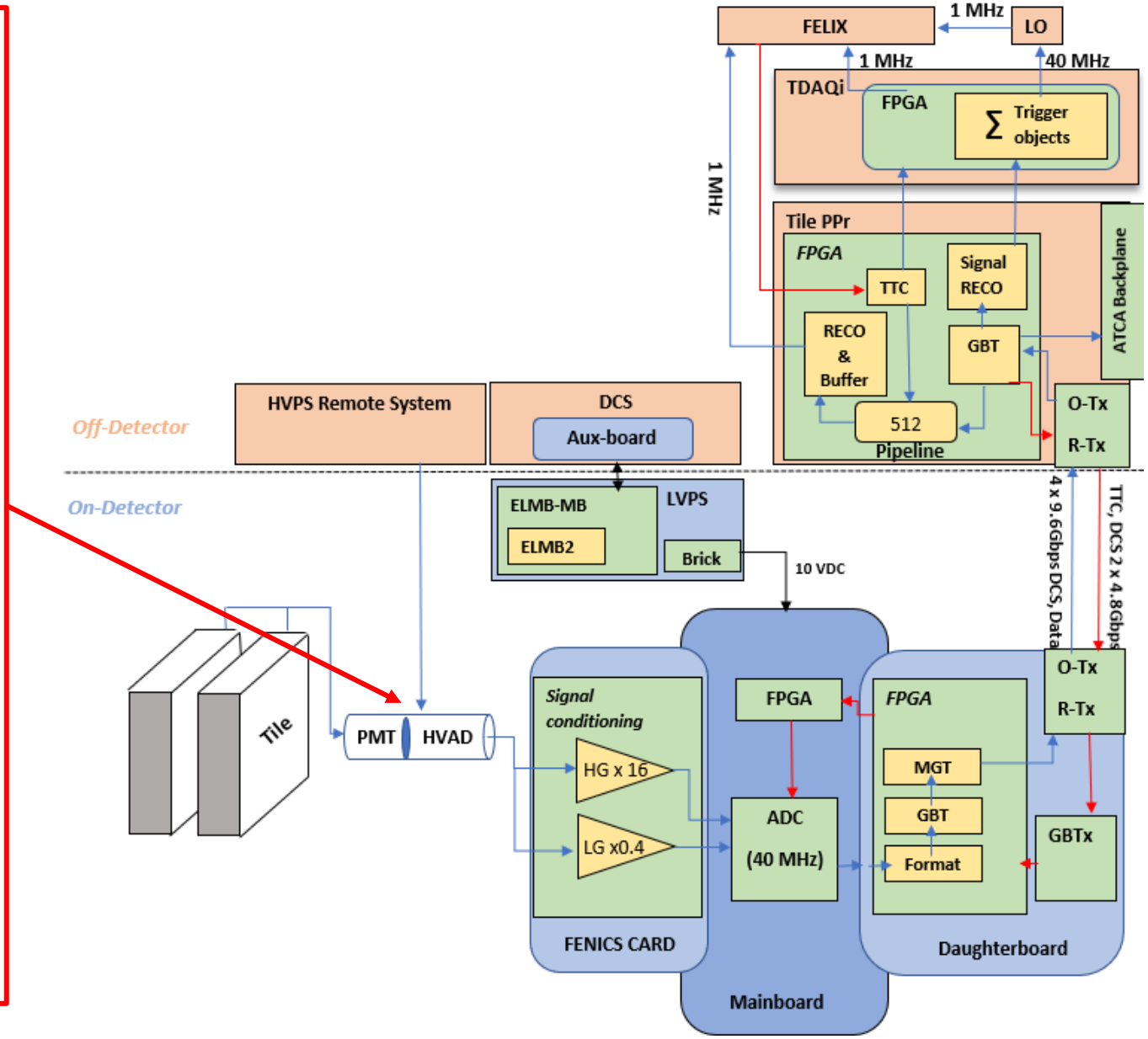


Fig. Super-drawer architecture designed explicitly for Extended Barrels modules, ATL-TDR-028 · LHCC-2017-019, pg 70

PMTs and High Voltage Active Dividers(HVADs)

- PMTs receive scintillation light via wavelength-shifting fibres. This light is then converted into electrical signals.
- A total of 768 PMTs located in the most exposed regions will be replaced due to aging.
- The HVADs make use of transistors and diodes in addition to passive components. They are responsible for dividing the received high voltage power between the individual dynodes of a PMT.
- The Upgrade ensures that the calorimeter performance, in terms of linearity and energy resolution for the measurement of highly energetic jets is maintained.



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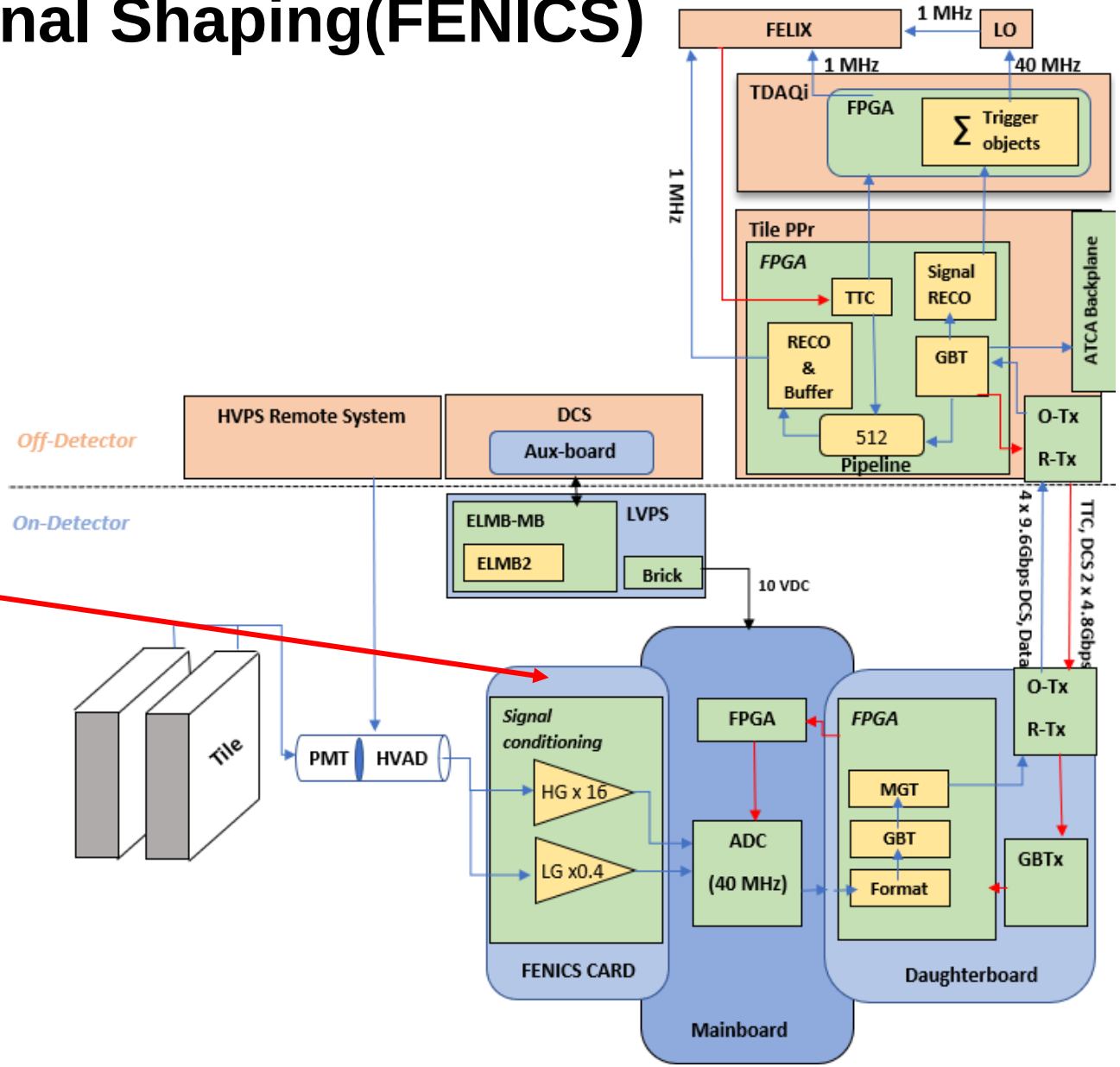
Front End board for the New Infrastructure with Calibration and signal Shaping(FENICS)

- A readout board responsible for the amplification and shaping of current received from a single PMT that is also involved in calibration as it contains the Charge injection system.
- FENICS reads the fast signals (full width at half maximum 25 ns) using two gains (x32, x1) and reads the averaged current (integration time 10ms) using six gains (0.3, 25, 25.3, 50.3, 125.3,150.3V/μA)



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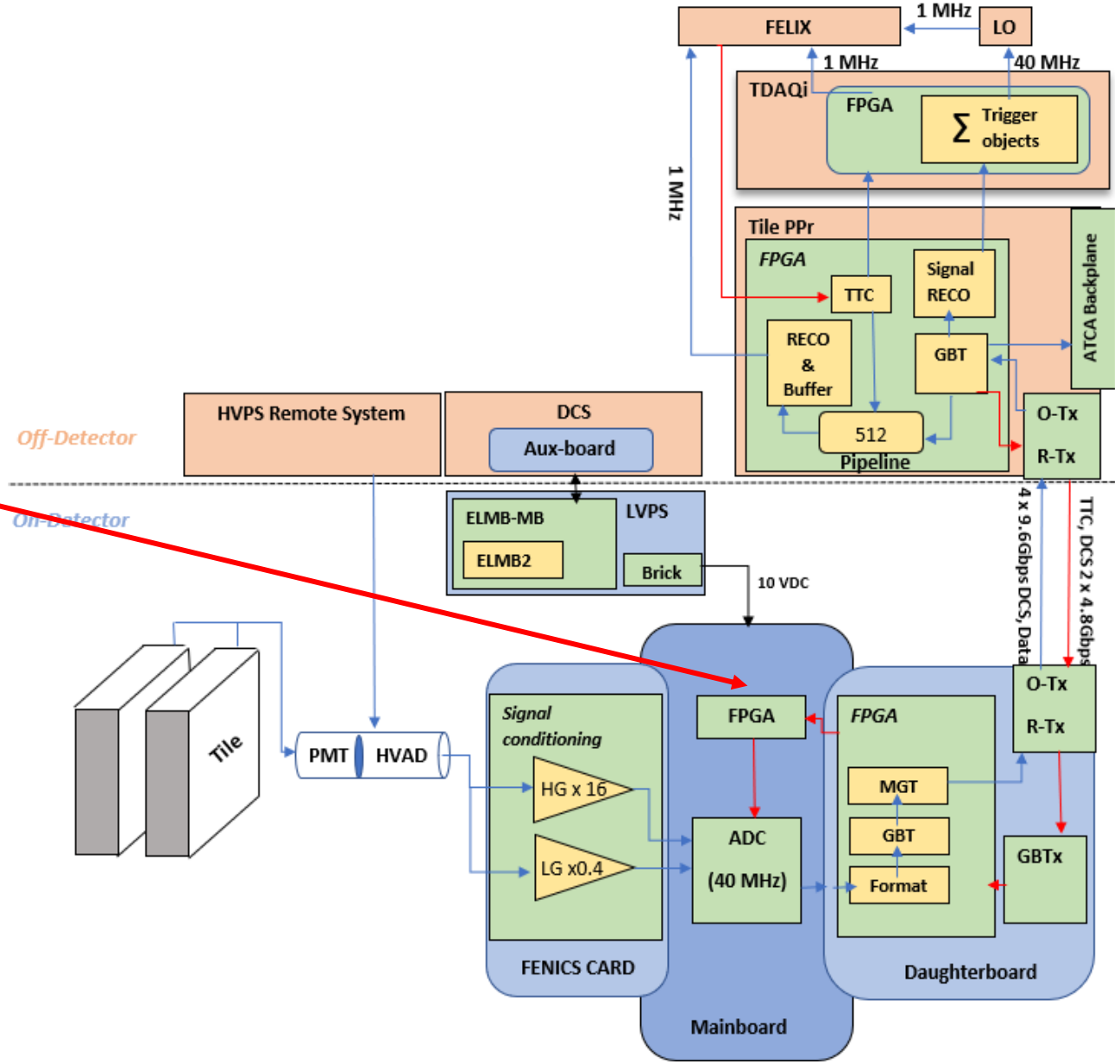
Mainboard (MB)

- There is an MB located in each Mini-drawer of TileCal. A single MB interfaces with twelve FEN-ICS and one DB. A MB digitizes the low and highgain signals received from the FENICS which arethen sent to its associated DB.
- An Upgraded MB is functionally divided into two halves for redundancy, provides digital control of the front end boards using Field-Programmable Gate Arrays (FPGAs), and features voltage and current monitoring.



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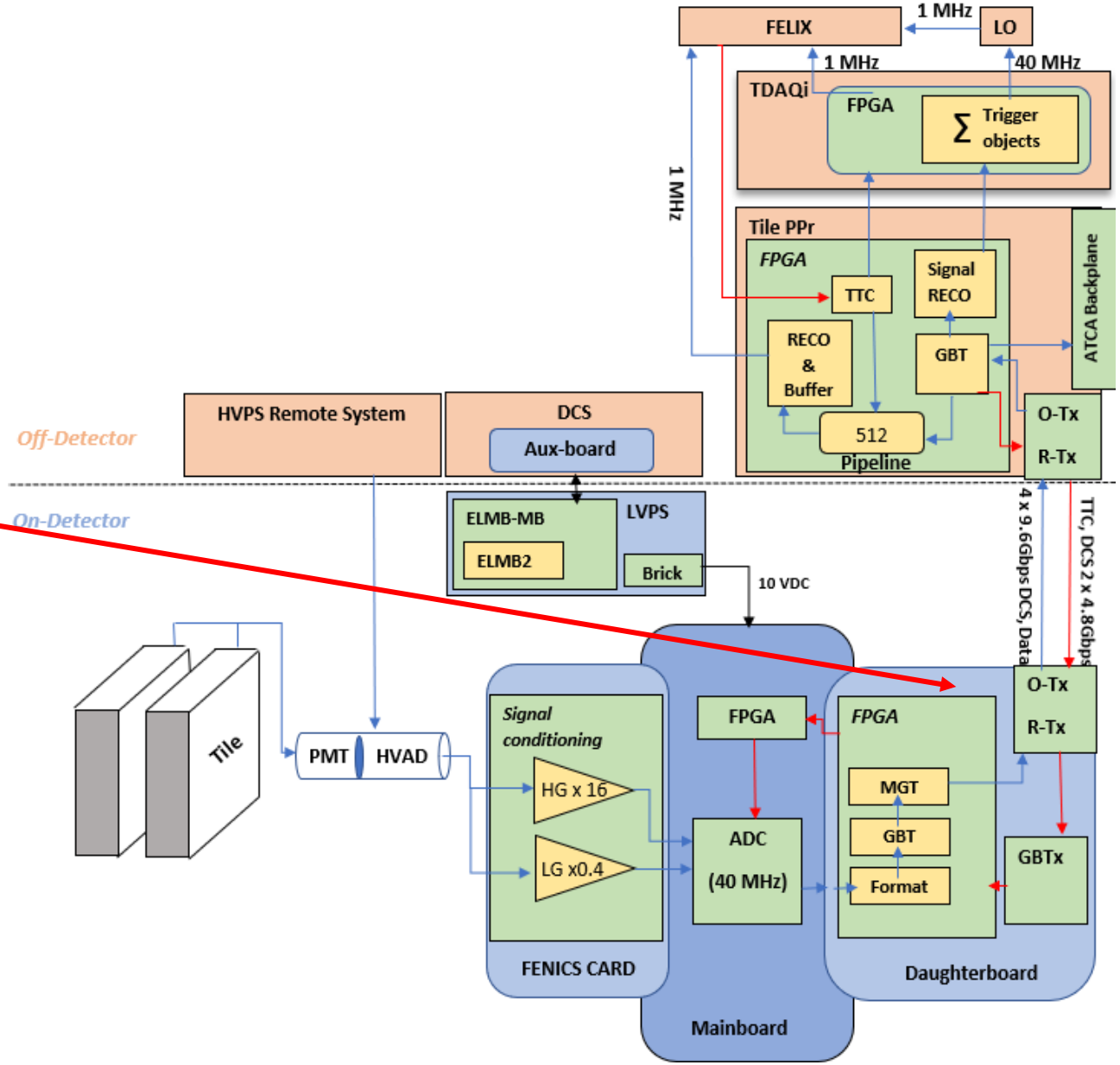
Daughterboard (DB)

- The DB is the primary interface between the on and off detector electronics of TileCal and is mounted on an MB. A DB sends detector data to the off-detector electronics, receives and distributes LHC clocks, configurations and slow-control commands.
- Major changes to the DB include using FPGAs with improved power sequencing as well as im-proved routing from the MB Analogue to Digital Converters (ADCs) to achieve better readout timing performance.



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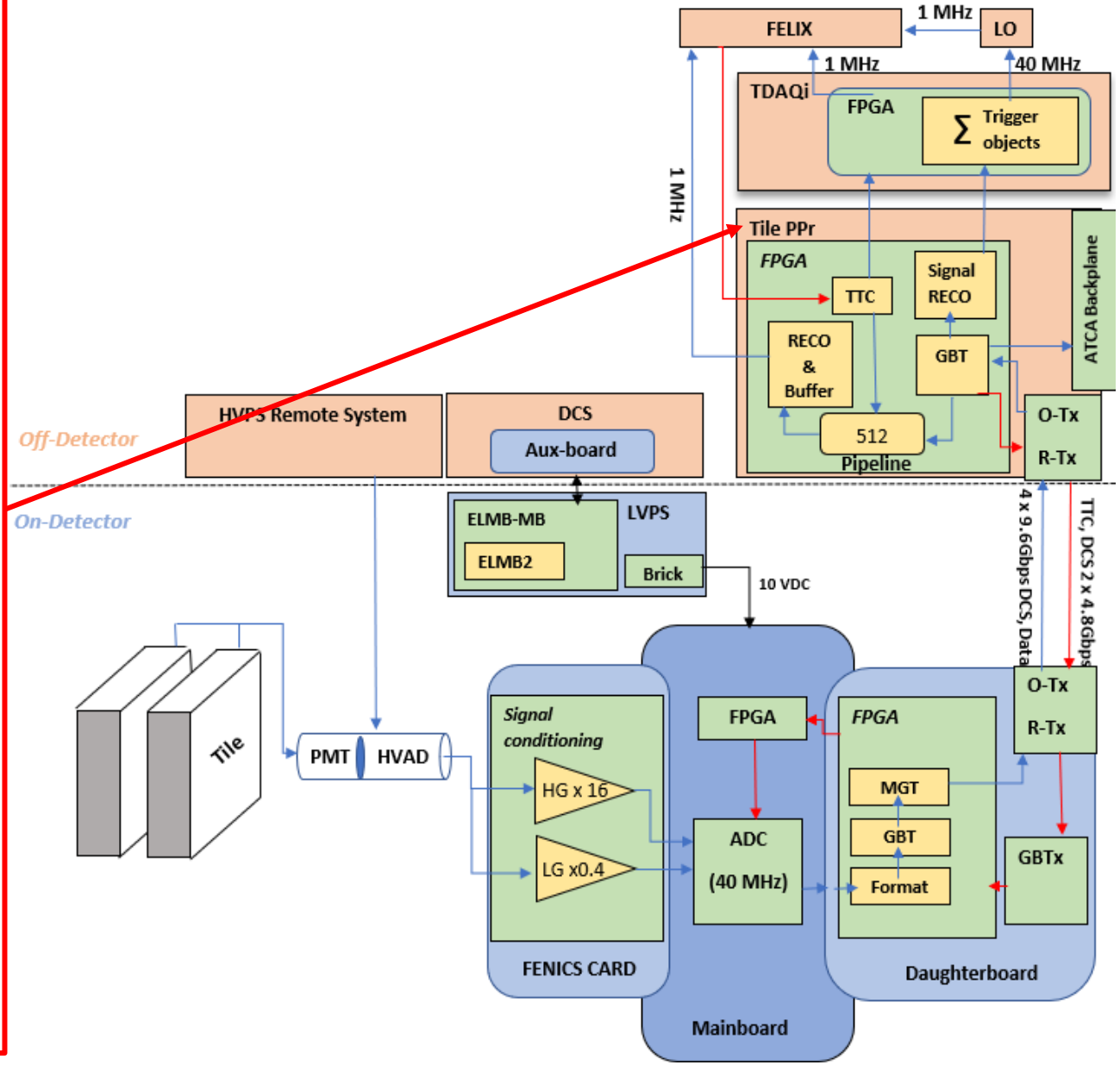
PreProcessor (PPr)

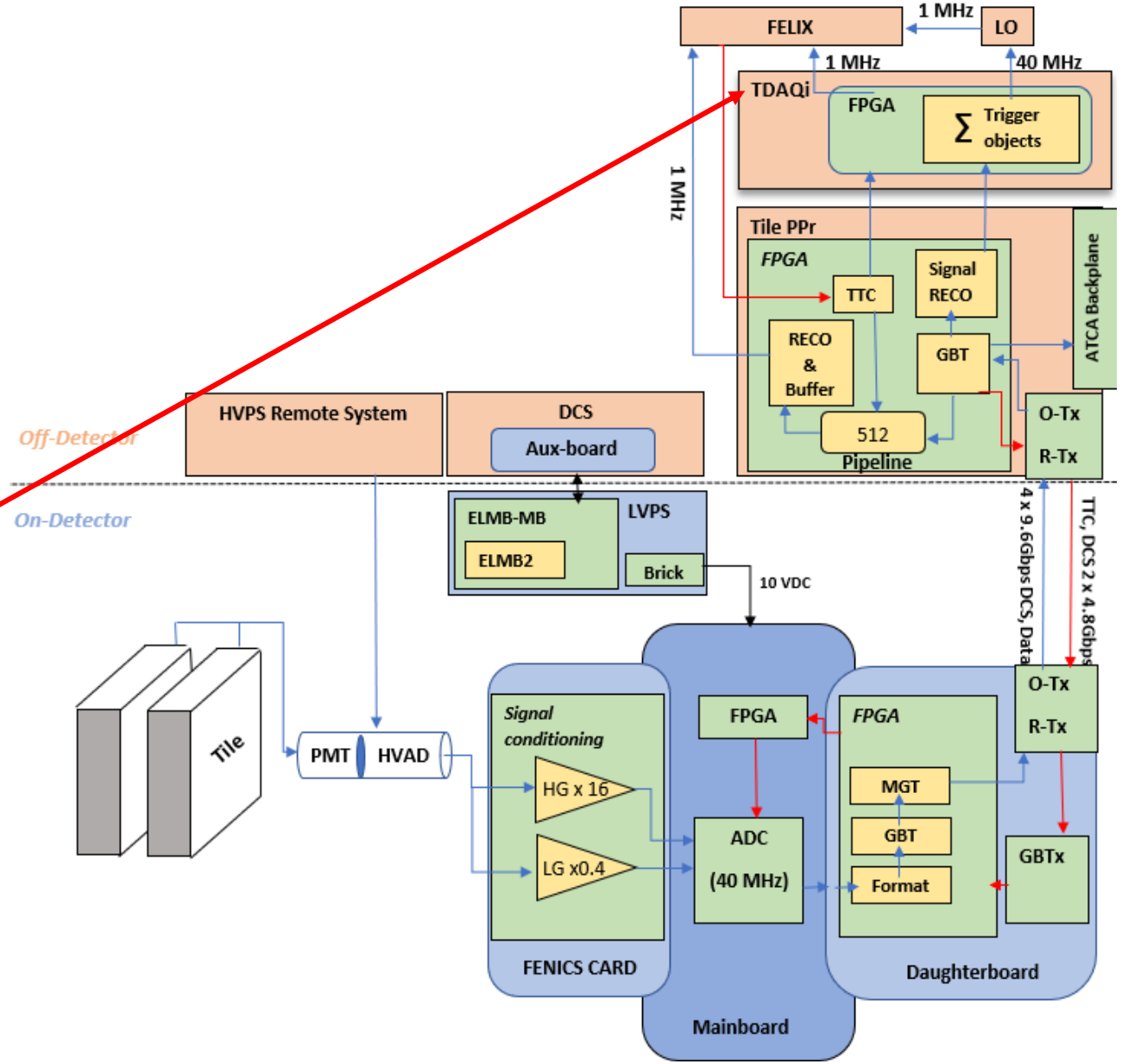
- A PPr is composed of four Compact Processing Modules(CPMs) and an Advanced Telecommunications Computing Architecture (ATCA) carrier board. Each CPM will read out and operate up to two TileCal SDs via high-speed optical links.
- A CPM implements a bi-directional GigaBit Transceiver communication with four 9.6 Gbps uplinks and two 4.8 Gbps downlinks per mini-drawer. The uplinks transmit detector and monitoring data to the CPMs. The downlinks provide Detector Control System (DCS) commands and Timing, Trigger, and Control information to the on-detector electronics, as well as the LHC clock for the sampling of the PMT signals.
- Deposited energy is reconstructed and calibrated in real-time using the received digitized samples. The CPM transmits this data to the TDAQi via the ATCA carrier board at the LHC frequency via four 9.6 Gbps optical links



MD: Mini Drawer
SD: Super Drawer
PMT: Photo multiplier Tube
FELIX: Front-End Link eXchange
TDAQi: Trigger and Data Acquisition Interface
FPGA: Field Programmable Gate Array
PPr: Pre Processor
ADC: Analog To Digital Converter
HVAD: High Voltage Active Divider
DCS: Detector Control System
ELMB: Embedded Local Monitoring Board
ELMB-MB: Embedded Local Monitoring Board Mother Board
HV: High Voltage
LV: Low Voltage
FR: Front End

Trigger and Data AcQuisition Interface(TDAQi)

- All interfaces between the TileCal and TDAQ are implemented in the TDAQi module.
- The TDAQi constructs the trigger primitives and interfaces with the trigger and FELIX systems.
- The Trigger FPGAs compute trigger objects for electrons, jet, global, and muon triggers and the results are transmitted through low latency high-speed optical links to the L0 trigger.
- Trigger sums changing from analog to digital.



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Low-Voltage Power Supply (LVPS)

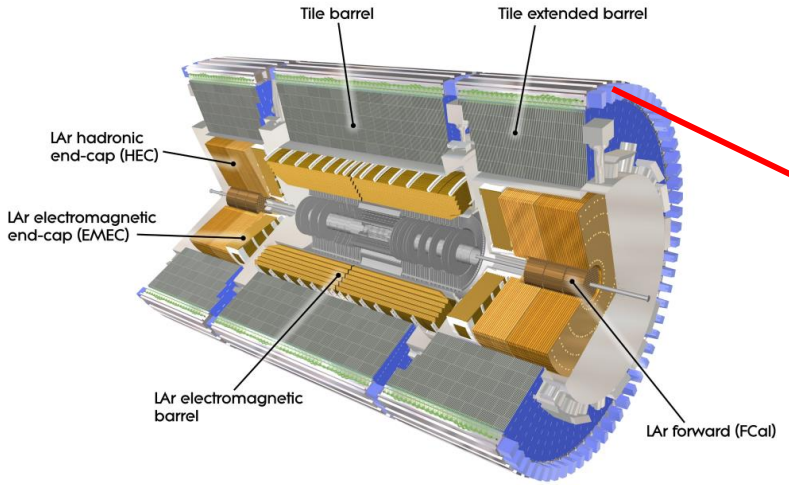


Fig. *The ATLAS Inner barrel*

X1

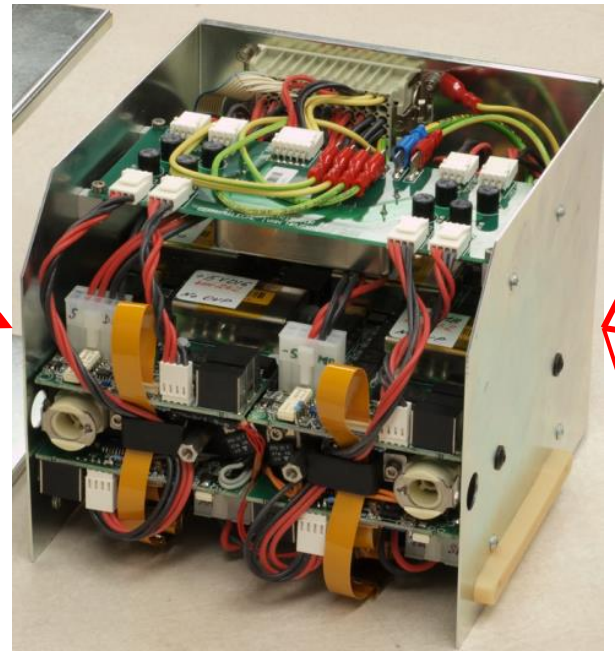


Fig. *Low-Voltage Power Supply*. ATLAS-TDR-028 pg 113

X1

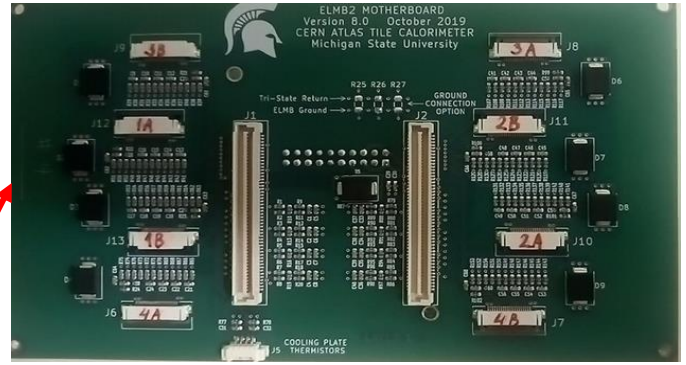


Fig. *Embedded Local Monitoring Board*

X8

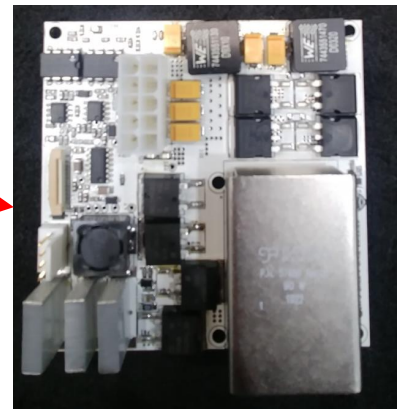
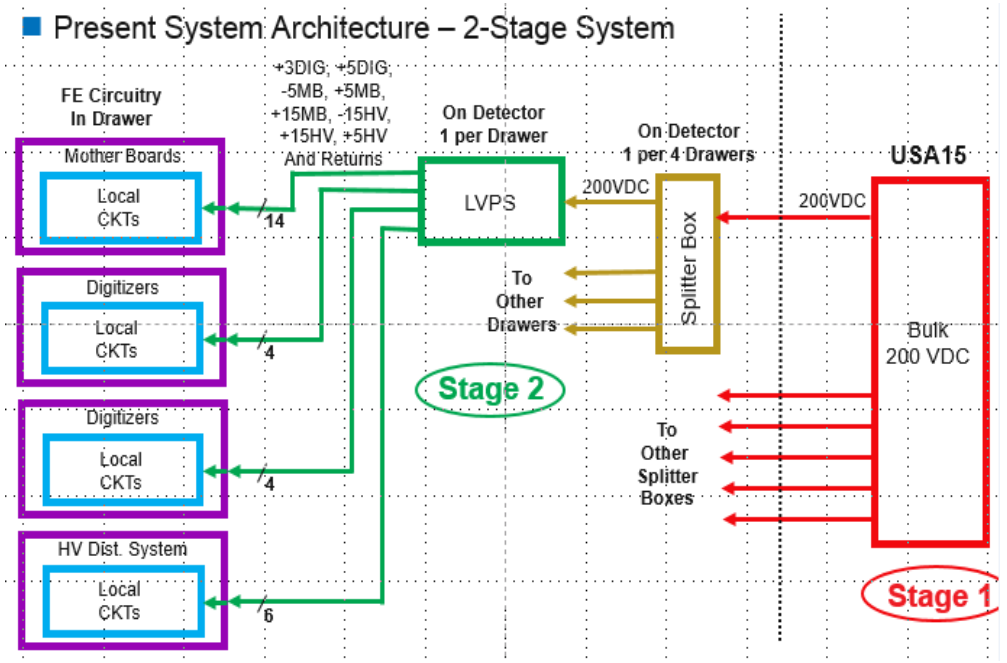


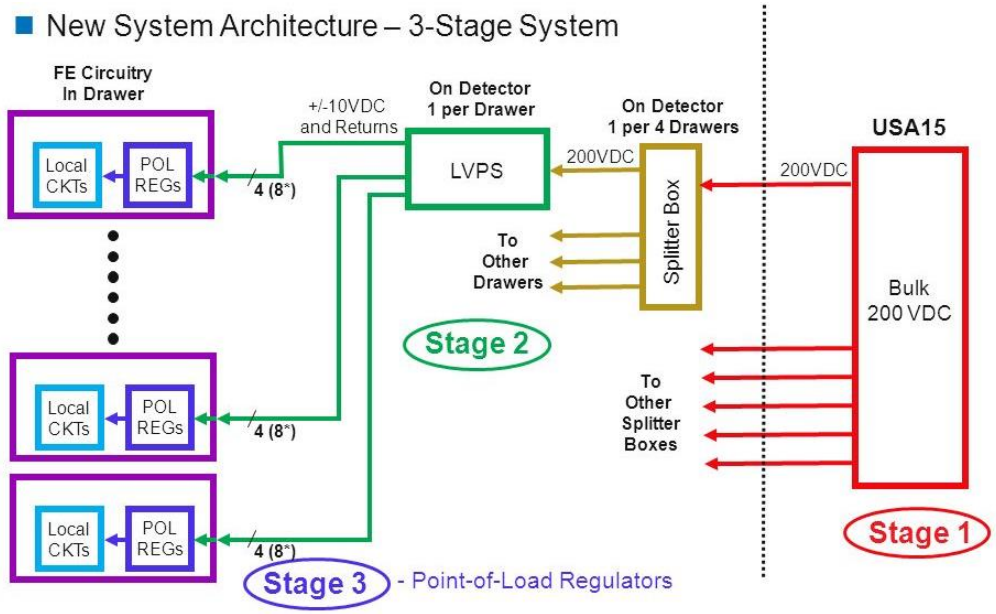
Fig. *South African High efficiency LVPS Brick top view .*

Fig. *Water cooled heat sink.*

Motivation for LVPS brick upgrade

- The main TileCAL upgrade pertains to the Front-End (FE) electronics: all data sent out is now digital, trigger signals are no longer analogue.
- Upgrade from a 2-stage to 3-stage power distribution system to accommodate the FE upgrades.
- Emphasis is placed on the reliability of the particle detector and by extension all of the subsystems and electronics therein
- LVPS's represent a single point failure in the readout system. – loss of data from a particular module.
- Limited access to LVPS on the order of once per year.





LVPS Brick functional block diagram

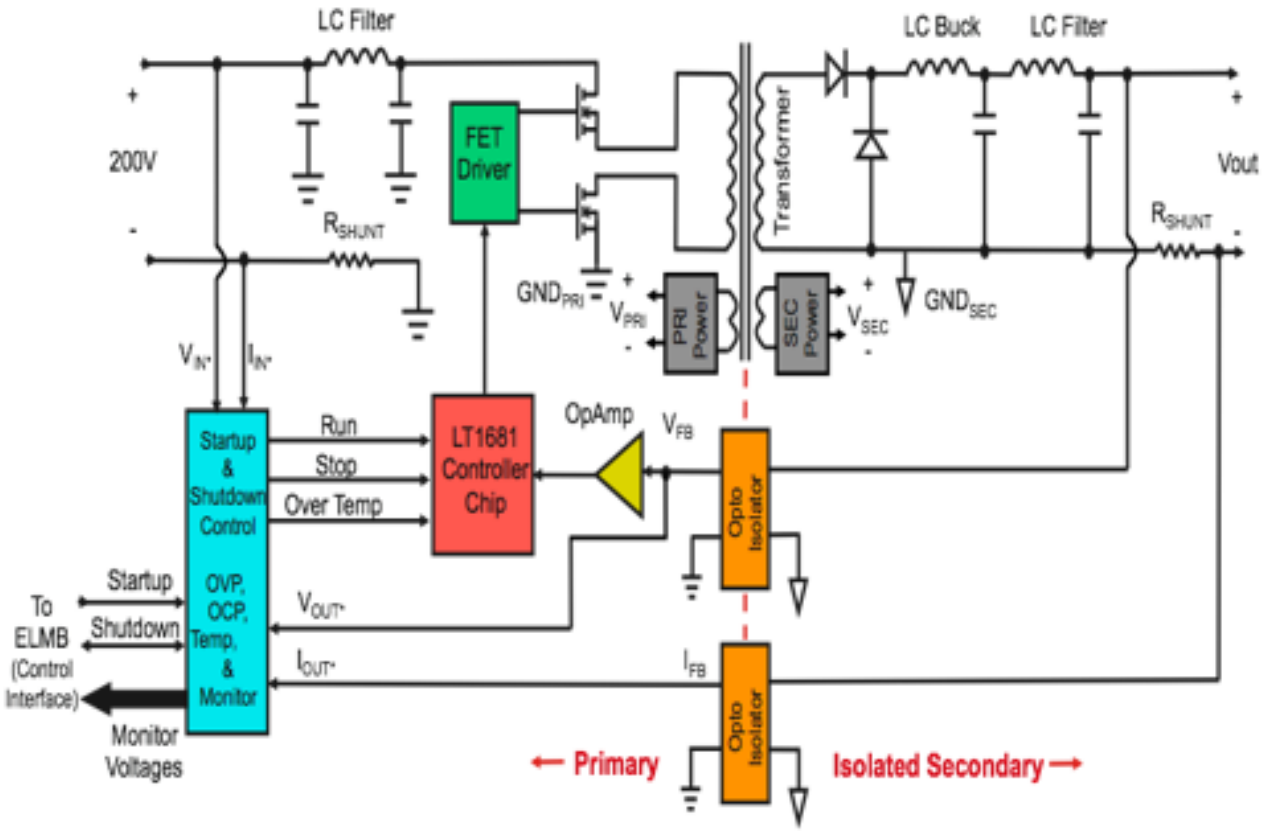


Fig. Block diagram of the LVPS Brick. ATLAS-TDR-028 pg 115

- LT1681 Controller Chip: Heart of design
- FET Drivers: Drivers which drive the Field Effect Transistors.
- FETs: When conducting current flows to the primary windings of the transformer which transfers energy to the secondary windings.
- Opto-Isolators: Provide voltage feedback for controlling the output voltage.
- Shunt Resistor: For measuring the output current
- Protection circuitry: Over Current Protection , Over Voltage Protection,

Initial Test Station Performance Metrics

Parameter	Minimum	Maximum
Frequency Standard Deviation	0	1000
Duty Cycle Standard Deviation	0	0.1
Frequency Max (Hz)	290000	350000
Frequency Min (Hz)	250000	310000
Minimum Stable Load (A)	2	2.1
Minimum Output Voltage (V)	9.8	10.2
Over Voltage Protection (V)	11.5	12
Over current Protection (A)	10.25	10.75
Output Root Mean Square Voltage	0	0.5
Clock duty cycle average	0	40
Clock Duty Cycle Standard Deviation	0	0.15
Start-up delay (Max) (s)	0.08	0.2

- Provide extrema of allowed operational environment of LVPS brick., i.e deviation about nominal.
- Based on operational limits of LVPS brick components.
- Over Voltage Protection (OVP),Over Current Protection (OCP) are very important.

LVPS Brick Burn-in station under construction

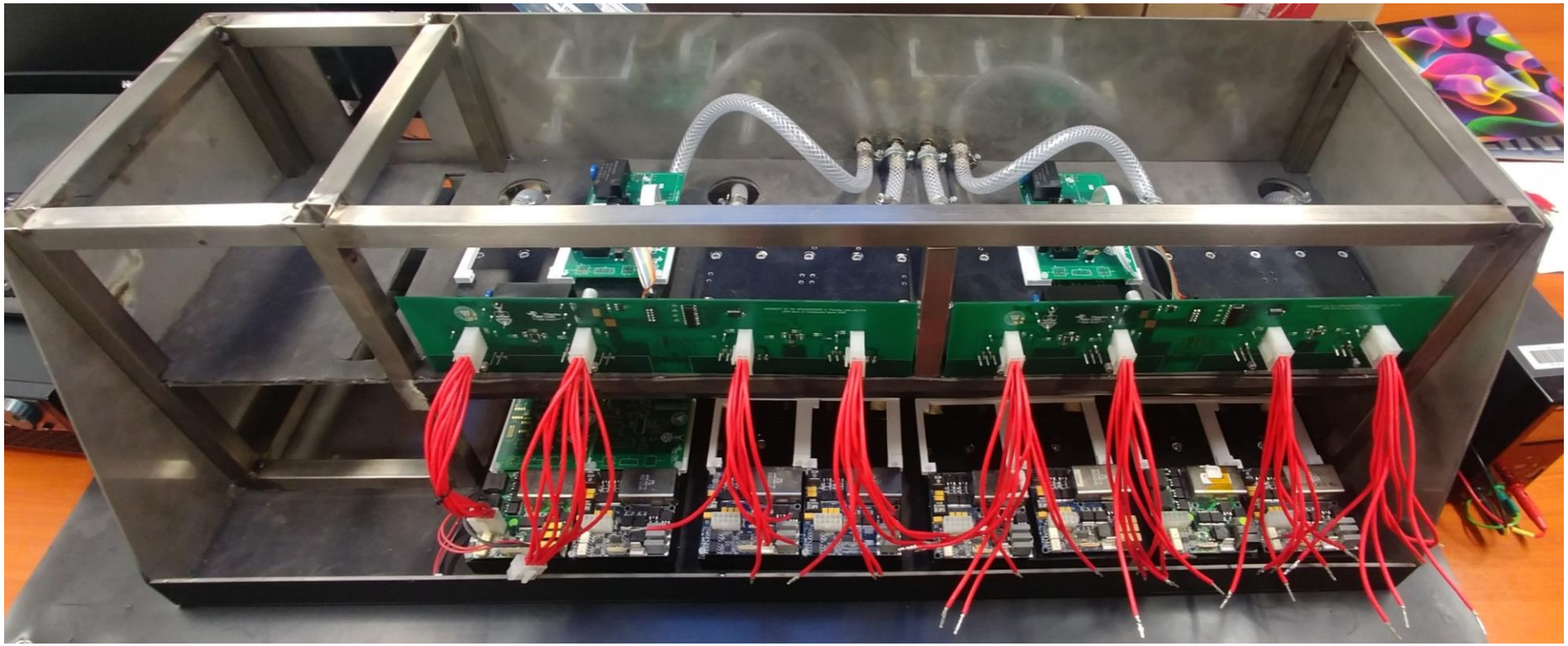


Fig. *LVPS Brick Burn-in station under construction.*

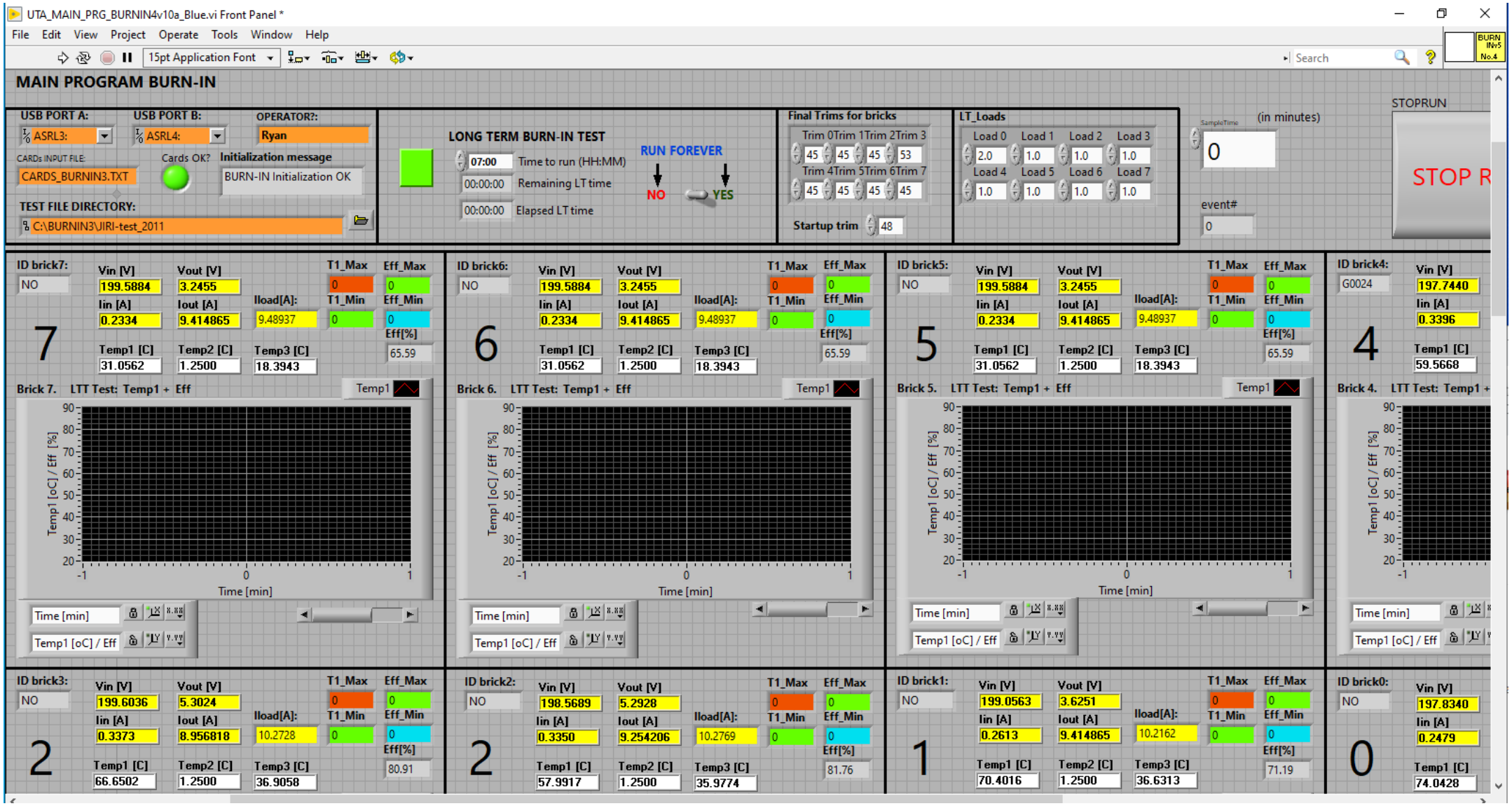
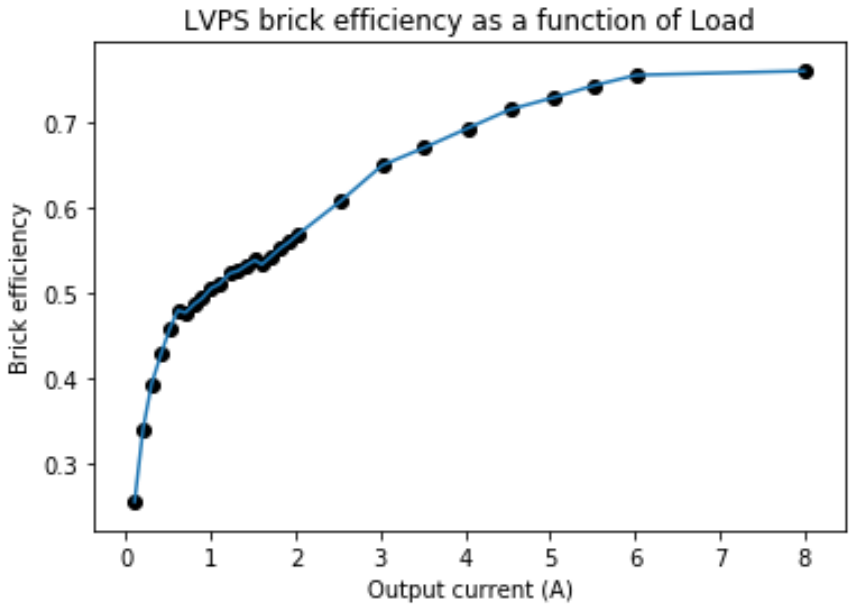
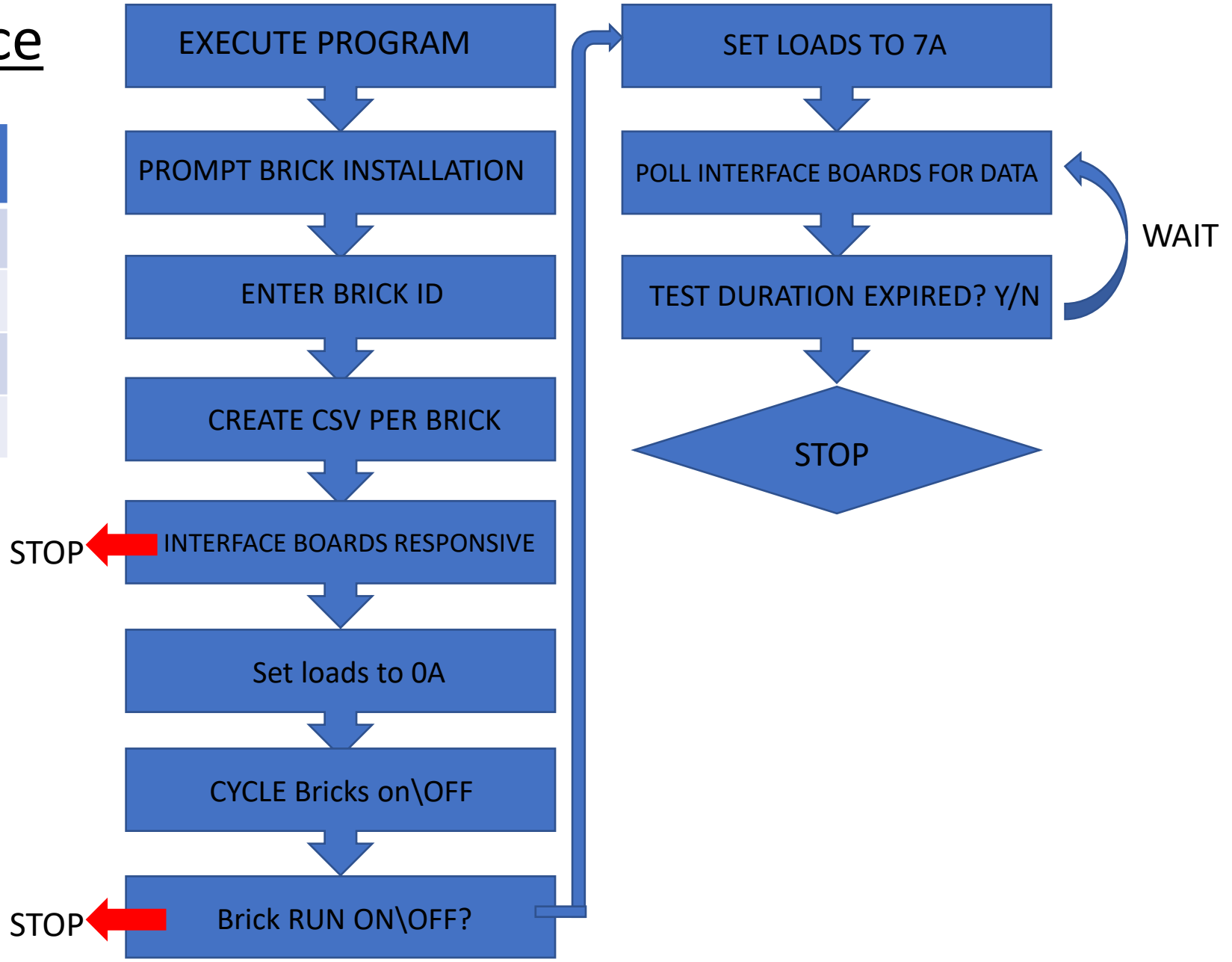


Fig. *Burn-in test station graphical user interface*

A Burn-in test sequence

Parameter	Value
Time duration	6 hours
Temperature	80°C
Brick Load	7A
Startup cycles	30+





Dummy-load board interfacing

Bypass mainboard using – UM232R

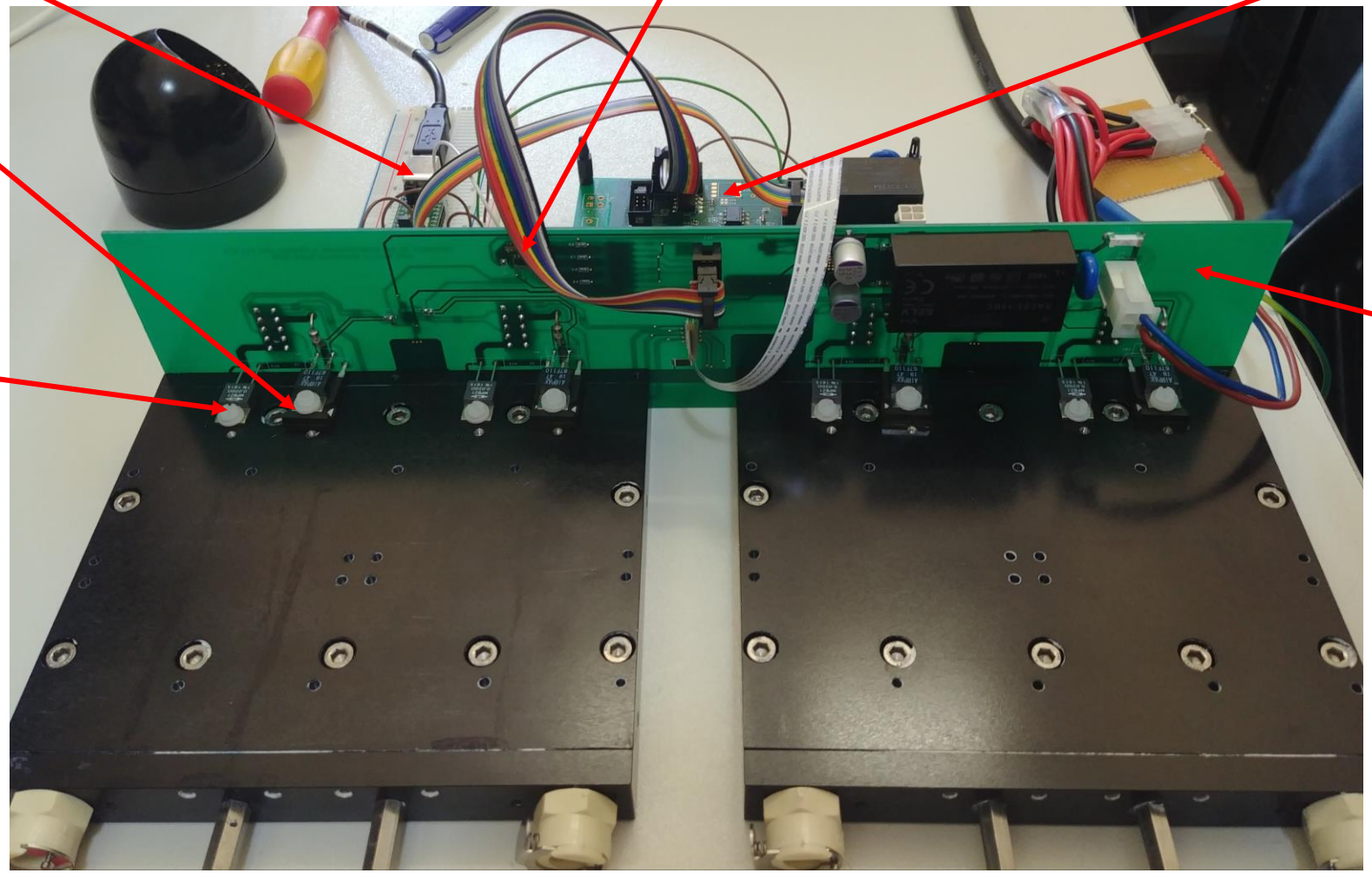
D1 Voltage regulator(Orientation is difficult to determine), text should be upright.

Load interface board

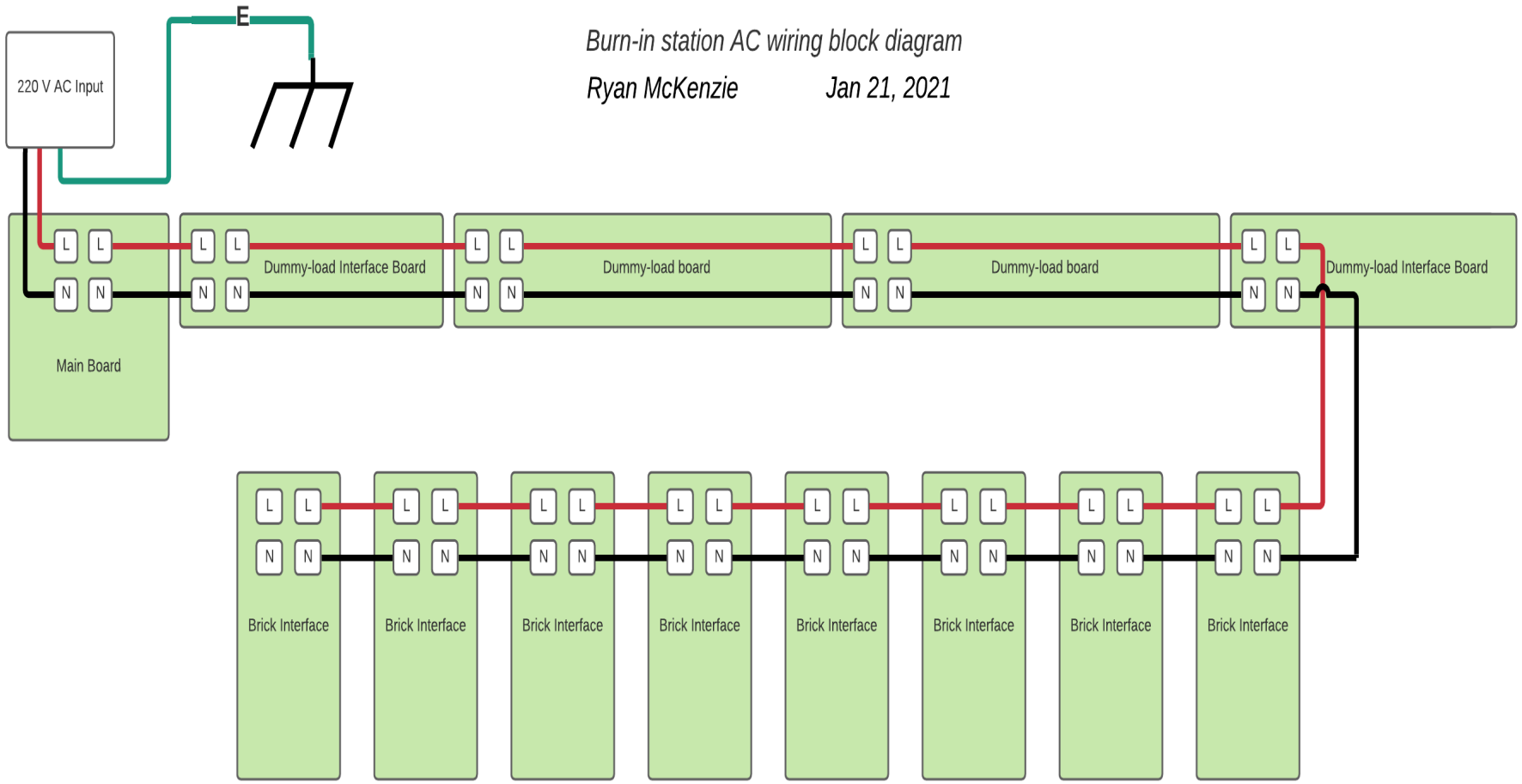
Mica insulation between plates and MOSFET

Nylon bolts

Dummy_load board



Brick Burn-in station AC Wiring Block Diagram

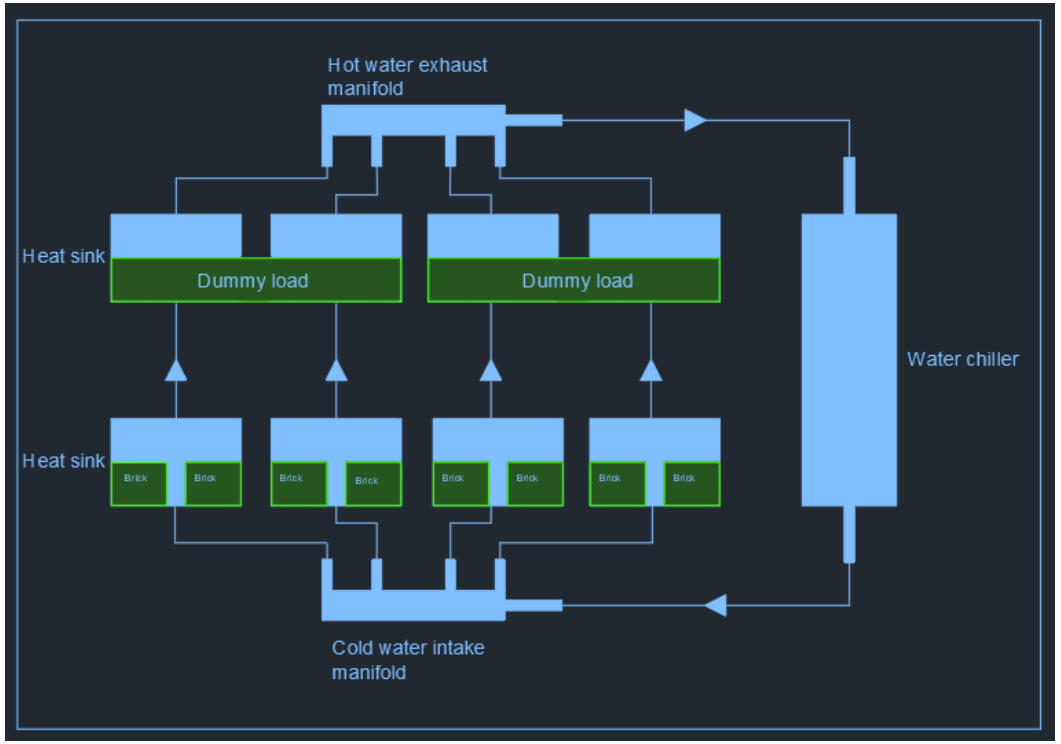


Burn-in station cooling block diagram

- Function: To extract heat from the dummy-loads and LVPS bricks.
- Considerations:

I. Total heat to be extracted ~ 750 W
II. Ensuring bricks receive 15°C coolant.
III. Require 86L/h per branch,
IV. Ensuring consistent flow rate.

- Additional flow meter to be added.



Water chiller

Water manifold