Firmware development for the upgrade of the Tile Calorimeter of the ATLAS detector

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Abstract. The Large Hadron Collider is scheduled to be upgraded in the year 2022, in order to increase its instantaneous luminosity. The High Luminosity LHC, also referred to as upgrade Phase-II, means an inevitable complete re-design of the read-out electronics in the Tile Calorimeter in which the completed new read-out architecture is expected to have the front-end electronics transmit fully digitized information of the full detector to the back-end electronics system. The back-end system will provide digital calibrated information with greater precision and granularity to the first level trigger, thereby resulting in improved trigger efficiencies. In Phase II, the current Mobile Drawer Integrity ChecKing (MobiDICK4) test-bench will be replaced by the next generation test-bench for the TileCal super-drawers, the new Prometeo (A Portable ReadOut ModulE for Tilecal ElectrOnics). The Prometeo's prototype is being assembled by the University of the Witwatersrand and installed at CERN for further developing, tuning and tests. This note presents some details on the design of the Prometeo, with particular emphasis on the firmware development for the Xilinx Virtex-7 XC7VX485T Field Programmable Gate Array (FPGA), which is the backbone of its VC707 motherboard. Some aspects are outlined on the VHDL hardware description language and the Xilinx Integrated Software Enviroment design suite which are employed in the firmware development.

1. Introduction

At CERN, the European Organization for Nuclear Research, the fundamental structure of matter is being probed by scientists and engineers. The Large Hadron Collider (LHC) accelerates and collides protons, and also heavy ions. The A Toroidal LHC Apparatus (ATLAS) [1] is one of two general purpose detectors used for detecting the sub-atomic particles produced during these high-energy collisions. The Tile Calorimeter (TileCal) [2] is the central hadronic calorimeter of the ATLAS detector. The year 2022 has been scheduled to see an upgrade of the LHC in order to increase its instantaneous luminosity. The High Luminosity LHC, also referred to as upgrade Phase-II, means an inevitable complete re-design of the read-out electronics in the TileCal [3] The completed new read-out architecture is expected to have the front-end electronics transmit fully digitized information of the full detector to the back-end electronics system. The back-end system will provide digital calibrated information with greater precision and granularity to the first level trigger, thereby resulting in improved trigger efficiencies and background rejection. The upper section of Figure 1 shows a schematic of the current front-end electronics while the lower section depicts the equivalent electronics set-up for Phase-II upgrade. In the current set-up, pipeline memories are used to store digitized data samples before they can be trigger-selected. The read-out electronics systems in each superdrawer are daisy-chained, resulting in

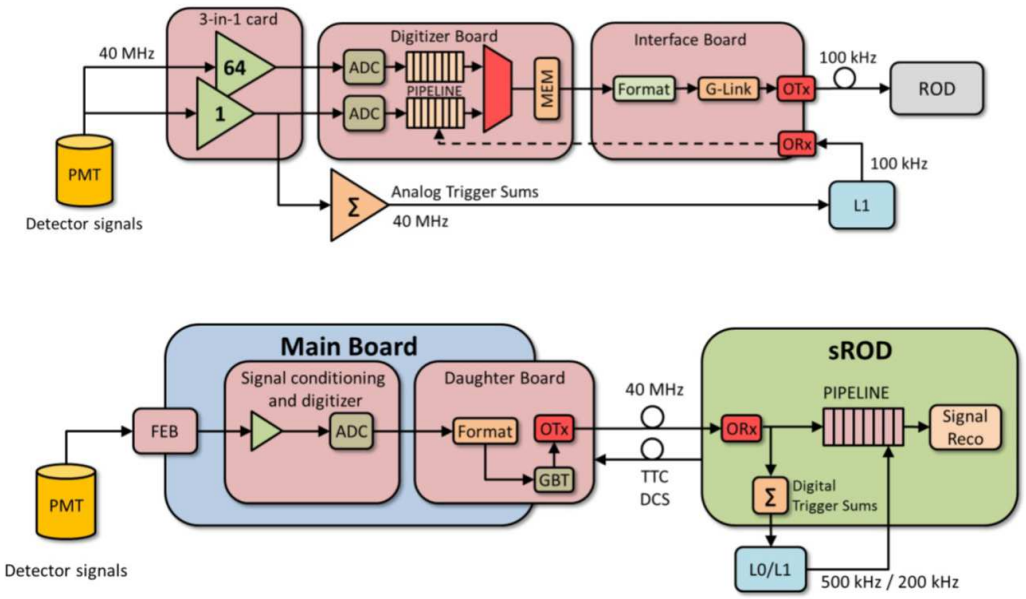

Figure 1. *Top*: Current front-end electronics; *Bottom*: Equivalent electronics for Phase-II upgrade.

the sharing of a data connection to the Read-Out Driver (ROD). In the future electronics design, each superdrawer has been divided into 4 minidrawers. One minidrawer hosts 12 PMTs and 1 daughter board. Each daughter board has one link to the super Read-Out Driver (sROD), thereby reducing failure rate by 25% with respect to ATLAS. There are up to 48 PMTs in one superdrawer, grouped in groups of 6 in a digitizer board. There are 16 digitizers for one superdrawer, interfaced by 1 interface card. It is envisaged that the future electronics will have:

- a super Read-Out Driver (sROD), capable of receiving data at 40 MHz as opposed to the current Read-Out Driver (ROD) which only handles 100 kHz,
- an increase in the number of point-to-point links with the front-end electronics,
- improved radiation tolerance,
- a higher read-out bandwith due to the need to read-out all sampled data to avoid corruption in the front-end pipeline memories.

An evaluation of this new proposed architecture is currently being carried out in the demonstrator project, where a small fraction of the detector (1/256) will be evaluated in test beams and inserted into ATLAS at the next shutdown of the LHC. In Phase II, the current Mobile Drawer Integrity ChecKing (MobiDICK4) system [4, 5] test-bench will be replaced by the next generation test-bench for the TileCal superdrawers, the new Prometeo (A Portable Read-Out ModulE for Tilecal ElectrOnics) [6]. The MobiDICK system faces challenges against aging and new technologies [7]. The Prometeo is designed to certificate the TileCal front-end electronics by performing multiple tests. The Prometeo's prototype is being assembled by the University of the Witwatersrand and installed at CERN for further developing, tuning and tests.

2. Prometeo

Figure 2 shows a schematic layout of the Prometeo. Prometeo has been designed to have the ability to: read-out all channels at the LHC bunch crossing frequency, assess the quality of data in real-time, diagnose malfunctions in each minidrawer, be self-contained and portable

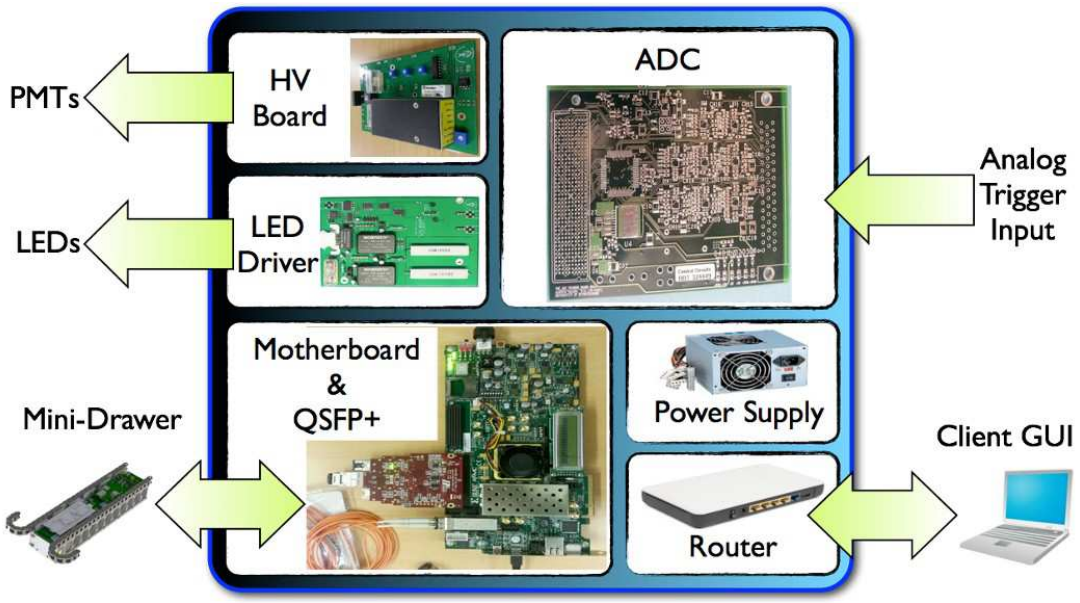

Figure 2. Schematic of the Prometeo.

for maintenance inside the detector, and be low-cost and scalable for network usage. Custom firmware is being developed for the FPGA for it to control and manage the data read-out. The Prometeo consists of several parts as follows:

- Main board: Xilinx VC707, Virtex-7 FPGA chip, 1 GB DDR3 RAM, two FMC connectors, received through SFP on the mainboard,
- Dual QSFP FMC card for digital communication with 2 minidrawers,
- Analogue to Digital Converter (ADC) FMC card: for the digitization of data in the hyprid demonstrator,
- High Voltage (HV) board: to turn on/off the HV and provide the -830 V voltage to power on the photo-multipliers (PMTs),
- Light Emitting Diode (LED) board: to illuminate the PMTs,
- Commercial ATX power supply,
- Ethernet router,
- Aluminum enclosure: whose dimensions are 50 cm $\times$ 35 cm $\times$ 20 cm in terms of length, width and depth, thickness of 3 mm and weight of 8 kg.

The design inherits features from the presently-used MobiDICK4 demonstrator. However, the latter makes use of a Xilinx ML507 evaluation board, with a virtex-5 FPGA. Figure 3 shows the upper and lower sides of the ADC board for Prometeo. This board was recently manufactured in South Africa. The LED and HV boards were also manufactured in South Africa.

3. Firmware development

The Xilinx Integrated Software Environment (ISE) design suite [9] is being used to develop firmware for FPGAs, where the coding language being used is VHDL. VHDL is the VHSIC Hardware Description Language, where VHSIC, in turn, stands for Very High Speed Integrated Circuit, which was a joint program between the US Department of Defense and IEEE in the mid-1980s to research on high-performance Integrated Circuit (IC) technology. The ISE design flow is illustrated in Figure 4. It comprises the following steps: design entry, design synthesis,

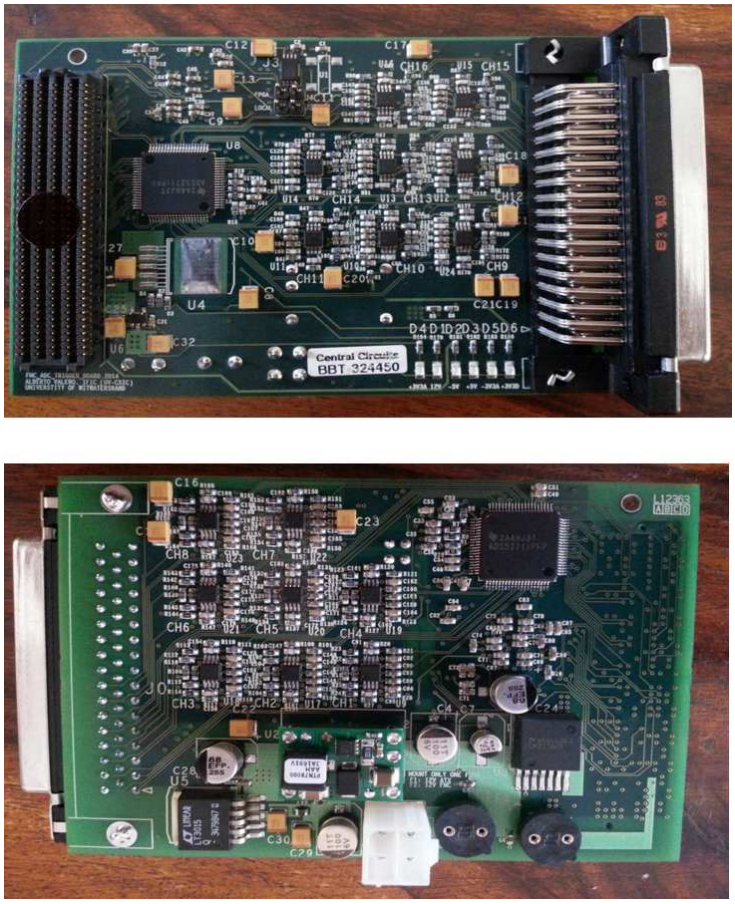

Figure 3. ADC board for Prometeo.

design implementation and Xilinx device programming. The design verification, which includes both functional verification and timing verification, takes place at different points during the design flow.

(i) **Design Entry:** One creates an ISE project in which files are created and added to the project, including a User Constraints File (UCF). Any existing files are assigned to the project at this stage. Timing constraints, pin assignments, and area constraints are also assigned

(ii) **Functional Verification:** One can verify the functionality of their design at different points in the design flow as follows: Behavioral simulation (also known as Register Transfer Level (RTL) simulation) is run before synthesis. Functional simulation (also known as gate-level simulation) is run after "Translate", using the SIMPRIM library. After device programming, one runs in-circuit verification. Behavioral simulation employs a high level of abstraction to model the design. A behavioral design might, for example, contain high-level operations, without containing specifics on how the design will be implemented. Synthesis tools then take these behavioral designs and infer the actual gate structures and connections to be used, generating a netlist description. Of the three simulation methods (behavioral, structural, and timing), behavioral simulation runs the fastest but provides the least design information. Behavioral simulation allows you to verify syntax and functionality without timing information. During design development, most verification is accomplished through behavioral simulation. Errors identified early in the design cycle are inexpensive

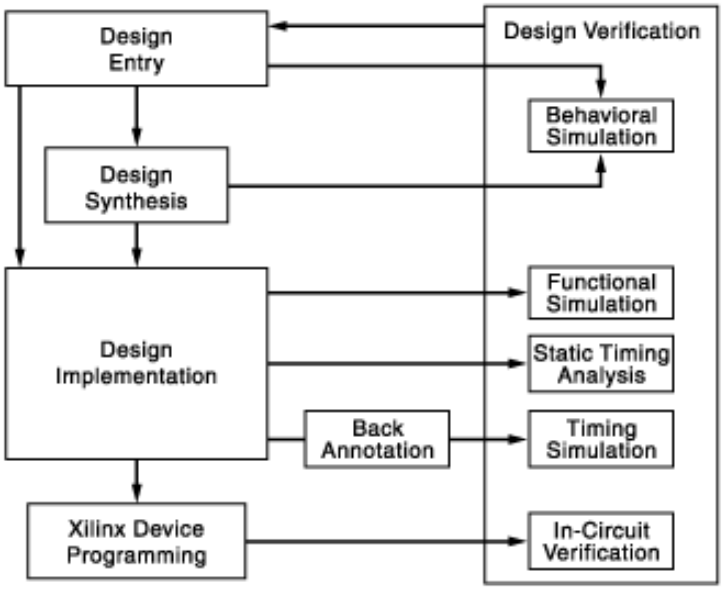

Figure 4. Integrated Software Environment (ISE) design flow.

to fix compared to functional errors identified during silicon debug. After the required functionality is achieved, structural and timing simulation methods can be implemented to obtain more detailed verification data.

(iii) **Design Synthesis:** After design entry and optional simulation, one runs synthesis. The ISE software includes Xilinx Synthesis Technology (XST), which synthesizes VHDL, Verilog,or mixed language designs to create Xilinx-specific netlist files known as NGC files. NGC files contain both logical design data and constraints. XST places the NGC file in the project directory and the file is accepted as input to the Translate (NGDBuild) step of the Implement Design process.

(iv) **Design Implementation:** After synthesis, one runs design implementation, which comprises the following steps:

- Translate - merges the incoming netlists and constraints into a Xilinx design file,
- Map - fits the design into the available resources on the target device,
- Place & Route - places and routes the design to the timing constraints,
- Generation of Programming File - creates a bitstream file that can be downloaded to the device.

(v) **Timing Verification:** One can verify the timing of their design at different points in the design flow by running static timing analysis after Map and after Place & Route. Timing simulations are performed after Map (for a partial timing analysis of CLB and IOB delays) and after Place and Route (for full timing analysis of block and net delays)

(vi) **Xilinx Device Programming:** This is done through creating a programming file (BIT) to program the target FPGA. The next step is to generate a PROM or ACE file for debugging or to download to one's device. Optionally, one may also create a JTAG file. Finally, one uses iMPACT to program the device with a programming cable.

The Prometeo firmware is being designed to perform both linearity and stability tests on each of the following:

- Charge Injection System (CIS)

- High Voltage (HV)
- Integrator
- Pedestal

These results are used for diagnosis of faulty PMTs, 3 in 1 cards, mainboards, daughter boards, optical links and analogue cards.

4. Conclusion

The Prometeo's prototype is being assembled by the University of the Witwatersrand and installed at CERN for further developing, tuning and tests. Firmware development for the Virtex-7 FPGA in Prometeo is ongoing, having been successfully completed for the Virtex-5 FPGA in the mobiDICK4 system and also for the Virtex-6 FPGA.

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