An ATCA framework for the upgraded ATLAS read out electronics at the LHC

Robert Reed

School of Physics, University of the Witwatersrand, Johannesburg, South Africa

E-mail: robert.reed@cern.ch

Abstract. The Large Hadron Collider at CERN is scheduled to undergo a major upgrade in 2022. The ATLAS collaboration will do major modifications to the detector to account for the increased luminosity. More specifically, a large proportion of the current front-end electronics, on the Tile Calorimeter sub-detector, will be upgraded and relocated to the back-end. A Demonstrator program has been established as a proof of principle. A new system will be required to house, manage and connect this new hardware. The proposed solution will be an Advanced Telecommunication Computing Architecture (ATCA) which will not only house but also allow advanced management features and control at a hardware level by integrating the ATCA chassis into the Detector Control System.

1. Introduction

The Large Hadron Collider (LHC) is situated between the boarders of France and Switzerland. Inside the 27 km ring two beams of protons are collided at very high energies. This is achieved by guiding the beam using superconducting magnets inside an ultra-high vacuum beam pipe. The proton packets are crossed every 25 nano seconds with 20 or more collisions happening at each instant.

This results in over 600 million collisions every second. To detect and identify the fragments in each collision, the ATLAS detector is sub-divided into numerous sub-detectors, each one having a specific function. Figure 1 shows the sub detectors of ATLAS. It consists of the Inner Detector, Electromagnetic Calorimeters, Hadronic Calorimeters and Muon Detectors. The Tile Calorimeter (TileCAL), shown in the central region, is designed to measure energies and directions of hadrons, jets, τ leptons. The TileCAL consists of plastic scintillators which, when particles pass through, emit light to photo-multiplier tubes (PMTs) which is digitized and passed on to where the first layer of triggering occurs. This happens on the front-end electronics.

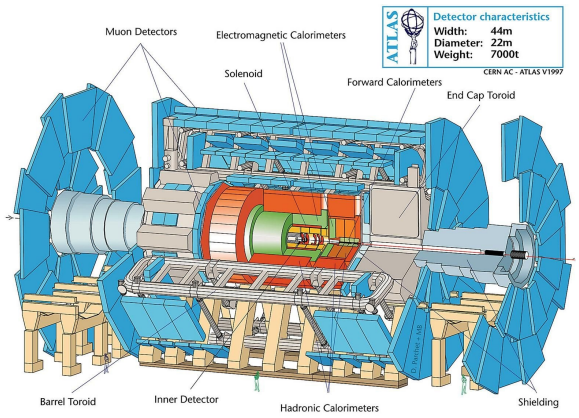


Figure 1. Representation of ATLAS detector showing structure of the sub-detector systems.

The front-end electronics are housed in superdrawers located on the outside of the TileCAL. If an event passes the triggering process, it is moved through to the Read Out Driver (ROD) to be sent to level two triggering. The ROD is located outside the detector in the back-end electronics inside a Versa Module Europa crate (VME crate). In order to meet the challenge of operating ATLAS at High Luminosity it is envisioned that the entire front-end electronics will be replaced [1].

1.1. Super Read Out Driver

The current front-end electronics consist of a long drawer which houses a 3-in-1 board, digitizer board and the interface board which packages the data for transmitting. Figure 2 shows the flow of data from the PMTs to the ROD. Data is generated at 40 MHz due to the number of bunch crossings per second and leaves the front-end electronics at 100 KHz to the back-end system.

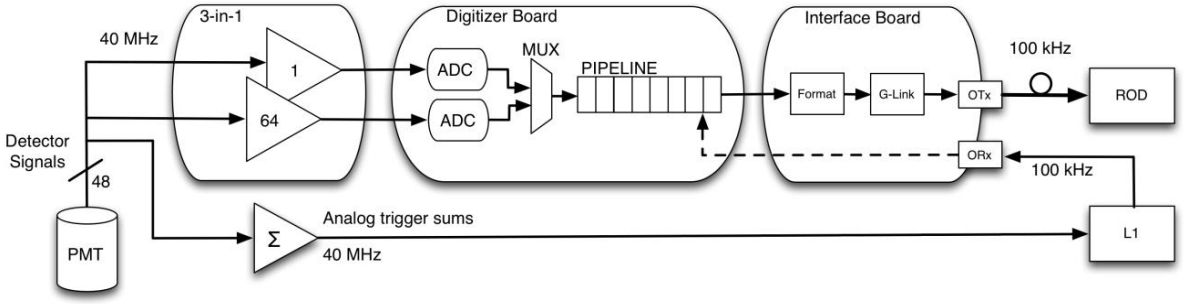


Figure 2. Current read out electronics.

During the 2022 upgrade the front-end electronics will be replaced with a new design. The triggering will become fully digital as well as being moved to the back-end but externally to the sROD. This will allow the full data rate of 40 MHz to exit the detector. Figure 3 shows the new data flow with the pipelines and triggering contained in the new super ROD (sROD) and accepting data at 40 MHz. Since the sROD is housed in the back-end it will be accessible during run time allowing easy maintenance and troubleshooting. Table 1 shows the expected bandwidth that will be provided by the new sROD and the TileCAL as a whole [2]. The sROD will be housed in an Advanced Telecommunications Computing Architecture (ATCA) chassis. The older VME crates will be phased out. The first prototype of the super Read Out Driver is currently in production. When it has been tested the designs for a revision board will be brought to South Africa where the PCB will be manufactured and all components mounted. The sROD will be inserted into the ATCA system at the University of the Witwatersrand and the integration with the WinCC software can be tested.

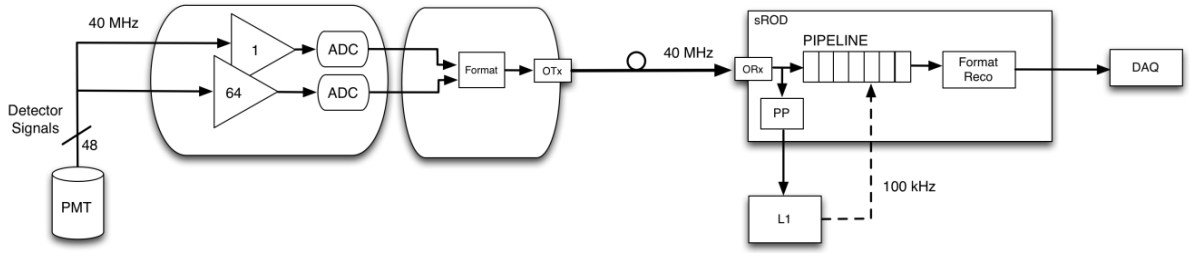


Figure 3. Upgraded read out electronics.

Table 1. Table Showing Bandwidth for Present and Future Design.

Phase	Present	Upgrade
Number of fibers	256	4096
Fiber Bandwidth	800 Mbps	10 Gbps
Total Bandwidth	205 Gbps	41 Tbps

2. ATCA Framework

The ATCA chassis is an intelligent shelf with high speed backplane connectivity. The chassis contains the backplane, power entry modules, fan trays and interfaces for individual blades to be installed. Figure 4 shows a front view of the chassis that is currently installed at the University of the Witwatersrand. This model has six slots with the first two connecting to all the others. This is called a dual star topology and offers the option of having a redundant switch installed. The connectivity is managed by a 10 Gbps switch module, providing routing and switching configuration. A carrier board provides power and monitoring to smaller Advanced Mezzanine Cards (AMC). The sROD is a doubled sized AMC card that can be inserted as shown in figure 4 (b). All boards can be "Hot Swapped" which means inserted or extracted while the chassis is still operational. The functionality is controlled by the Shelf Manager which provides various methods of accessing and controlling the devices such as the Simple Network Management Protocol (SNMP). The ATCA follows the PCI Industrial Computer Manufacturers Group (PICMG) standard. PICMG, as defined on their website, is "a consortium of companies who collaboratively develop open specifications for high performance telecommunications and industrial computing applications." [3].

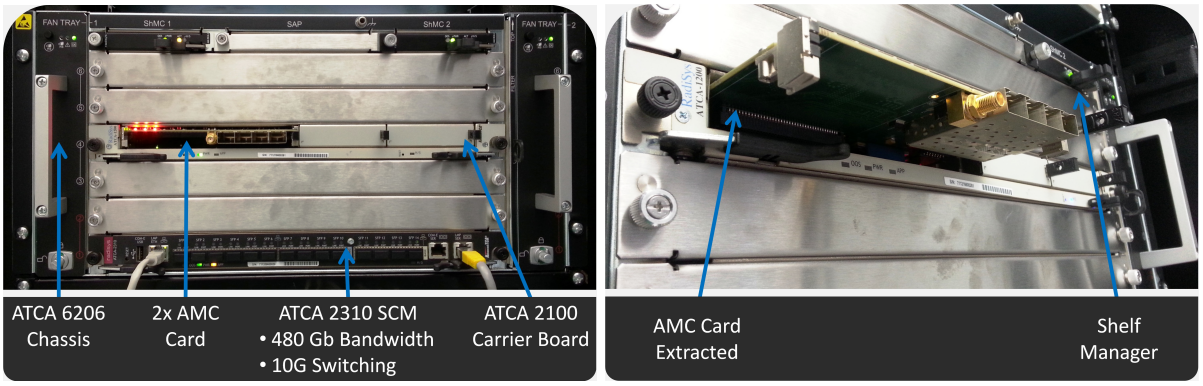


Figure 4. a) Front of ATCA chassis and b) AMC extracted from chassis at Wits.

3. Integration into the Detector Control System

The ATLAS Detector Control System (DCS) is a complex system of hardware monitoring drivers arrange in tiers according to geographic, function or dependency groups. The software used at CERN is called WinCC Open Architecture designed by Siemens [4]. The suggested channel to insert the ATCA system can be seen in figure 5. The demonstrator setup will be installed in the Long Barrel A Partition of the TileCAL.

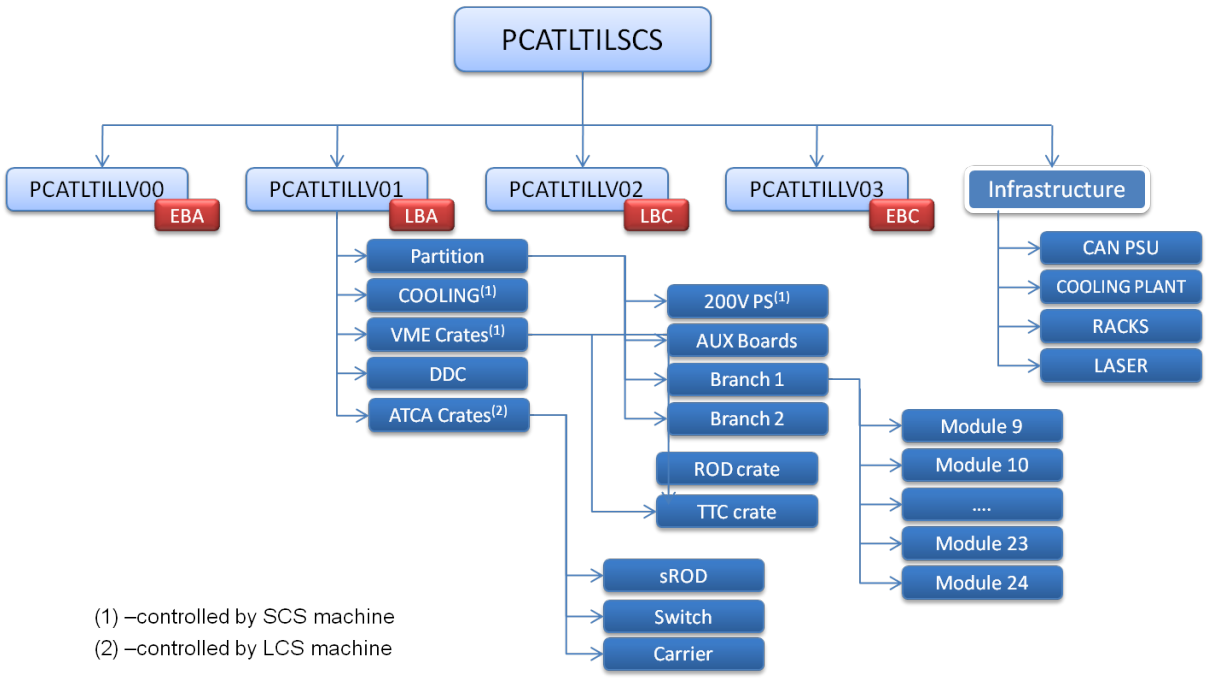
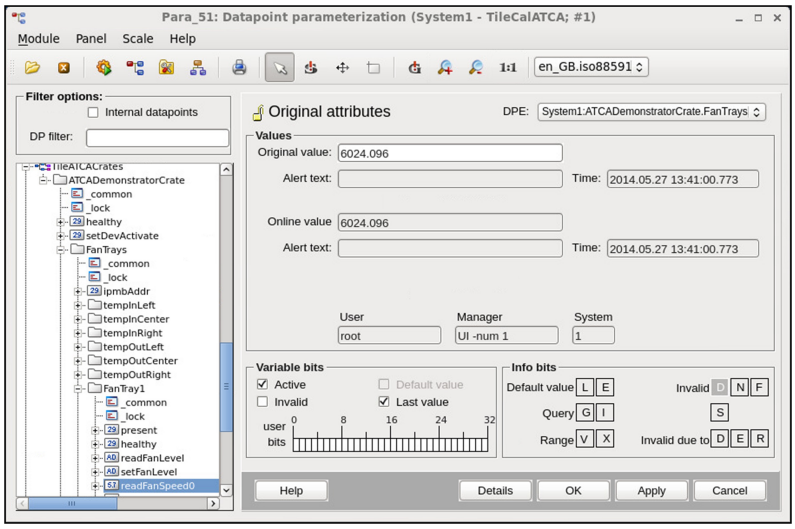


Figure 5. Proposed channel in DCS structure for ATCA Crates.

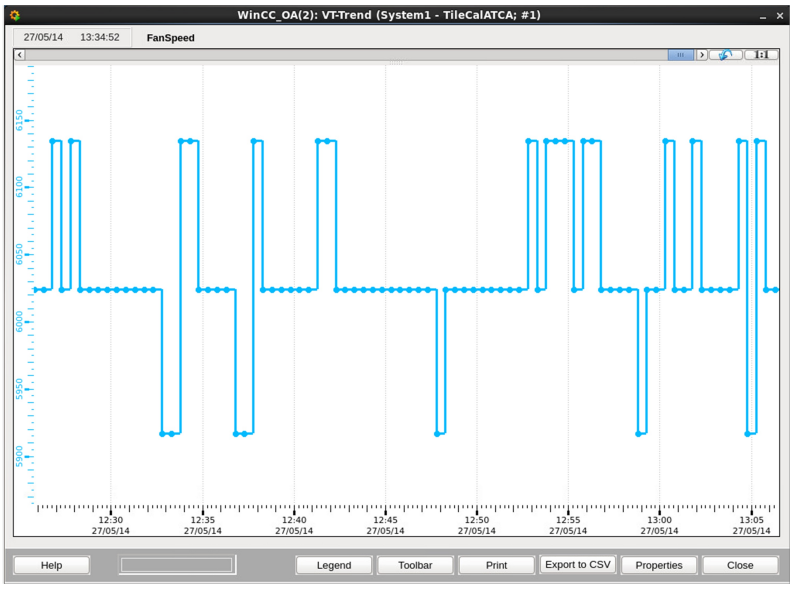
In order to properly integrate the chassis with the DCS system, all variables of interest in the sROD and ATCA chassis must be actively polled to provide the relevant information. The design will use SNMP to retrieve sensor readings via a standard Ethernet connection. This simplifies the infrastructure setup as Ethernet is common, cheap and understood. SNMP is a set of standards for network management which includes a list of data objects to monitor, a database to store and a protocol layer for communication. The device to manage is the ATCA chassis and all modules inserted. The internal control and management of modules is done by the ATCA shelf manager which acts as an SNMP agent. The WinCC software is the network management layer which retrieves information and issues commands to and from the SNMP agent via a standard Ethernet cable. A single variable has been successfully integrated into the WinCC software. The data point structure can be seen in figure 6 (a) which includes all variables of the ATCA. These data points were generated by a script which automates the creation process to make it easier to add more chassis. Figure 6 (b) shows the successful archiving of a single fan speed sensor represented as a trend over a few minutes.

4. Conclusions

The CERN community will be adopting the new ATCA and μTCA systems to replace the majority of the current VME crates in future upgrades. The work up to now has facilitated the understanding of these new systems. It has been shown that this new SNMP approach does work while using a protocol that is common and already understood. The integration into the DCS system, although not quite plug and play, is possible due to the inbuilt SNMP features in WinCC. The future work will entail script writing to automate a large amount of the work as well as design control scripts to automatically respond to certain events. This work will need to be thoroughly tested before the final integration into the ATLAS DCS.



(a)



(b)

Figure 6. a) Data point structure of ATCA crate and b) Trend graph of single fan speed sensor.

Acknowledgements

The University of the Witwatersrand has facilitated the research by purchasing the required hardware to allow hands on development for this work and for other big science applications. The National Research Foundation (NRF) is thanked for the bursary they provided. The SA-CERN program provided financial assistance for research visits to CERN. I would also like to thank the School of Physics, the Faculty of Science and the Research Office at the University of the Witwatersrand.

References

[1] The ATLAS Collaboration 2012 Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment URL `http://cds.cern.ch/record/1502664?ln=en`

[2] Carrió F, Ferrer A, Castillo V, Hernández Y, Higón E, Fiorini L, Mellado B, March L, Moreno P, Reed R, Solans C, Valero A and Valls J A 2013 *ATLAS Note, The sROD Module for the ATLAS Tile Calorimeter Phase-II Upgrade Demonstrator* URL `http://cds.cern.ch/record/1628753?ln=en`

[3] PICMG PICMG - About Us URL `http://www.picmg.org/v2internal/aboutus.htm`

[4] Siemens 2014 SCADA System SIMATIC WinCC - HMI Software URL `http://www.automation.siemens.com/mcms/human-machine-interface/en/visualization-software/scada/Pages/Default.aspx`