High-speed data playback of VLBI hardware correlator

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Abstract VLBI(Very Long Baseline Interferometry) is an important radio astronomy technology, is widely used in deep-space probers high-precision measurement. The correlator as the core data pre-processing equipment of VLBI, its performance is very important. At present, China VLBI data acquisition system (CDAS) can collect data 2Gbps, and multiband combination can reach 16/32Gbps. For ensure the requirements of high-speed and high-precision, there used Uniboard as the hardware platform, used 10G Ethernet as the data playback interface and 1G Ethernet as the control interface, research the VLBI data playback which speed up to 4Gbps for single CDAS, and design some pre-processing method just like data correct and data decode specific to the VLBI data characteristic. Now we have finished the preliminary system, and there will show the design and some results.

Keywords VLBI, Hardware Correlator, data playback, high-speed

1 Introduction

VLBI(Very Long Baseline Interferometry) is an important radio astronomy technology, is widely used in deep-space probers and high-precision measurement. We have successfully used it to perform VLBI observations for serveral Chang'E mission[1].Figure 1 is the Chinese VLBI Center architecture. The VLBI center is comprised of VLBI stations, Data preprocessing, Correlator, POST correlator, SKD, Orbit, Location, etc. Hardware correlator is the VLBI core data pre-processing equipment, can calculate important parameters such as : the delay, delay rate, correlation amplitude, interferometric phase and so on.

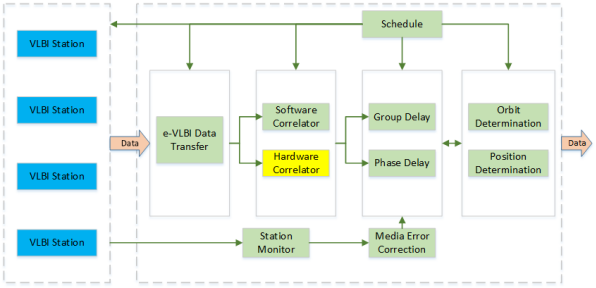

Fig. 1 Chinese VLBI Center

Already in use, the hardware correlator have 5 FPGAs which configured in two columns. The front column contains 4 FPGAs to process 4 stations data, the back column contains 1 FPGA which process all channels data from 4 stations at the same time. So the speed of system be confined. Now, our team used the Uniboard as the hardware platform. The UniBoard, as the name suggests, is a universal processing platform which will be used on multiple processing application like future EVN correlator and so on. The board exists of 8 processing FPGAs configured in two columns. The front column contains the front nodes, these FPGA are each connected to four 10GbE SFP+ inputs making copper and optical interfacing possible. Via mesh on the board a front node is connected to each back node with a 10Gbps link. The backside or back node FPGA are connected to a backplane. The control of the board is done via an onboard 1GbE switch with four copper

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interfaces on the front panel and eight 1GbE connection one for each processing FPGA[2].

2 VLBI Data Playback System

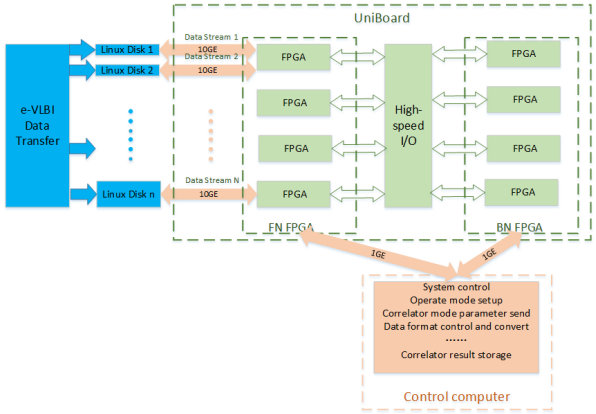

Fig. 2 Uniboard Hardware Correlator system

In Figure 2 a block diagram of Uniboard showing the connections can be seen[3]. The system has characteristic like:

- 8 processing FPGAs are divided into 4 front FPGAs and 4 back FPGAs
- One station can correspond to one 10GbE interface, so each front FPGA can design 4 stations at most.
- 4 back FPGAs synchronous processing all channels data, that can processing data more quickly
- 1GbE not only be used to control every board, but also be used to send the result data to control computer.

VLBI Date Playback include 10GbE interface, data playback control module, date receiver and memory, strip-head module, cross switch, fan in, SOPC, 1GbE interface[4]. In Figure 3, the 1 means 10Gb Ethernet interface initialize and control parameters, the 2 is playback parameters, include reset, start time, stop time, fan-in code, data bit , FFT size and so on, the 3 means send frame header information to control computer real-time to ensure the time synchronization.

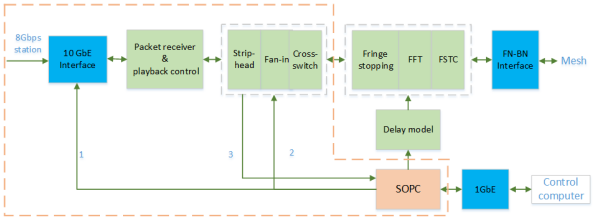

Fig. 3 One station Front FPGA

2.1 10GbE module

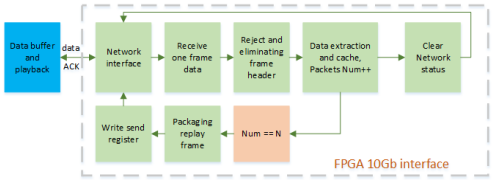

Fig. 4 FPGA 10G interface

The 10GbE Network module include 10GbE interface, data playback control module, used to receive data, cache data and control data playback. The Figure 4 is the 10GbE communication and control block diagram. It using an ACK to control the data playback start or stop, processing is:

- Linux disk send N packets to FPGA via 10GbE, and waiting replay packet
- FPAG receive N packets and the post-processing is not full, then send a replay packet to the Linux disk .
- Linux disk receive the ACK packet and send data packets continue, if not then waiting until received.

In theory, the speed of data transmission is 10G per second for no load, and can reach to 8Gbps for preprocessing, but just to 4Gbps in fact.

2.2 SOPC

SOPC system is the bridge of the embedded software core system and hardware IP module, to keep data communication on both sides. The embedded software system NiosII main function:

- Receive and analysis the network packets, write data to corresponding hardware IP module.
- Receive data from hardware IP module, process and send to control computer.

The 1GbE is used to receive data from control computer and send data to aim computer. The 1GbE receive parameters packages for each processing FPGA and send confirmative information. And send result to PC when trigger TX data mode. The 1GbE Ethernet transmission has two operation modes:

1. RX-TX mode. Receive the 1GbE packets at first, and send replay packets after.
2. TX only. Package and send data to control computer under control.

And the Figure 5 show the RX-TX mode working state.

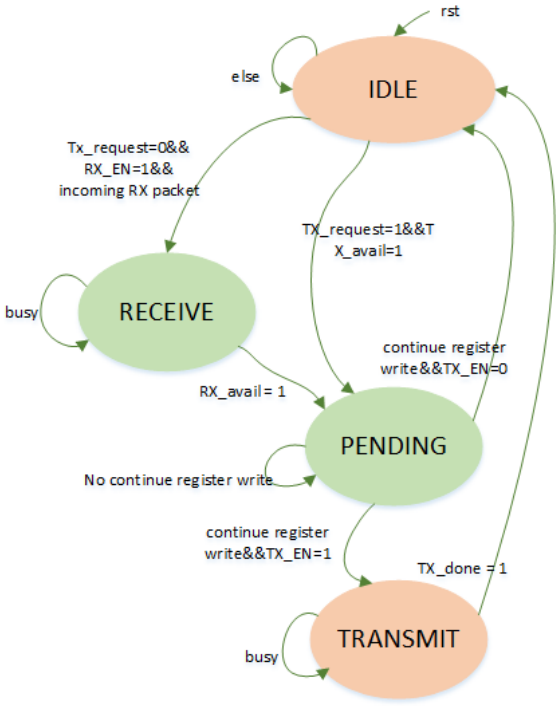

Fig. 5 1GbE RX-TX mode

3 Analysis

The Figure 6 is the result of Correlation on real-time, the data from the CE5-T1(Chinese Lunar Mission), and there are 4 stations but the pictures show 2 stations only. Compare with real-time mission, the result is the same current Correlator.

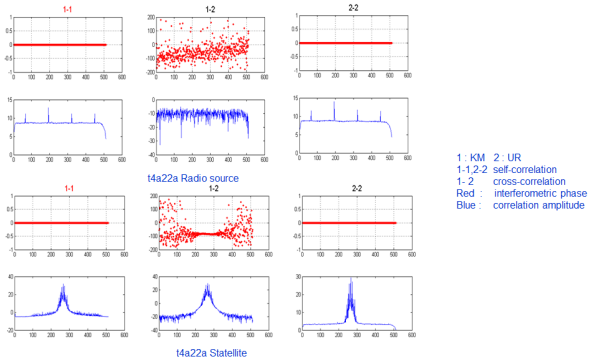

Fig. 6 Result of Correlation

4 Conclusions

The Uniboard correlator has already been finished and has some characteristic show in table.

Mode	Near Real-time	Real-time
10GbE Interface	4Gbps	8Gbps
IO Interface	6.25Gbps	6.25Gbps
Delay Tolerate	20s	1s
Buffering	Disk	Memory
Design Difficulty	10GbE,high speed IO	DDR3,System
Applications	Deep space exploration	VGOS,SKA

However, there still have some ability need to be improved, and more astronomical application will be added.

5 Future plan

As an near real-time style correlator, the data latency need less than 25 seconds during the CE-3 mission[5], and the stations less than 5. So there still need more

working to meet more requirements for new mission, just like:

- Support 4, 8 and 16 bit sampled data
- VDIF, VSR format data playback
- Support more stations(6/8 or more)
- Multi-target processing
- Multi-bandwidth processing
- Add DDR3 to cache data

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