An electronics test-bench for the certification of the Tile Calorimeter of the ATLAS detector

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Abstract. The instantaneous luminosity of the LHC at CERN is envisaged to be increased by up to 5-7 times after its upgrade in the year 2022. Termed the upgrade Phase-II, the High Luminosity LHC will bring with it a mandatory complete re-design of the read-out electronics in the Tile Calorimeter of the ATLAS detector. Here, the new read-out architecture is expected to have the front-end electronics transmit fully digitized information of the detector to the back-end electronics system. This will allow more sophisticated reconstruction algorithms which will contribute to the required improved trigger efficiencies at high pile-up. Currently, the MobiDICK test-bench is being used to test the front-end electronics of the TileCal. The MobiDICK will be replaced by a new test-bench for the new Phase-II electronics. The new test-bench is being designed, developed and assembled by the University of the Witwatersrand and installed at CERN to gain experience with prototype electronics. The new PROMETEO is a portable, high-throughput electronic system for full certification of the new front-end electronics of the ATLAS TileCal. A description is given in this article, of the overall design of the new PROMETEO, and its crucial role in TileCal electronics upgrade.

1. Introduction

The European Organization for Nuclear Research, well known as CERN, is a research organization that operates the largest particle physics accelerator in the world, the Large Hadron Collider (LHC). The LHC accelerates and collides protons, and also heavy ions. ATLAS [1] is one of two general-purpose detectors at the LHC. It investigates a wide range of physics, from the search for the Higgs boson to extra dimensions and particles that could make up dark matter. The Tile Calorimeter (TileCal) [2] is the central hadronic calorimeter of the ATLAS detector. Alternating steel plates and plastic scintillator tiles make up each cell of TileCal. The energy of the detected particles is sampled by the scintillators and signals are collected from the photomultipliers (PMTs) by the front-end electronics located in super-drawers, which is the outermost part of the detector.

The readiness of the TileCal for data collection is determined by testing each of its modules, hence, the need for an electronics test-bench. The High Luminosity LHC will lead to an inevitable complete re-design of the read-out electronics in the TileCal. Figure 1 shows a comparison of the current and future front-end electronics set-up for the TileCal. In the current front-end, pipeline memories are used to store digitized data samples before they can be trigger-selected. The read-out electronics in each super-drawer are daisy-chained, resulting in the sharing of a data connection to the Read-Out Driver (ROD). In the future electronics

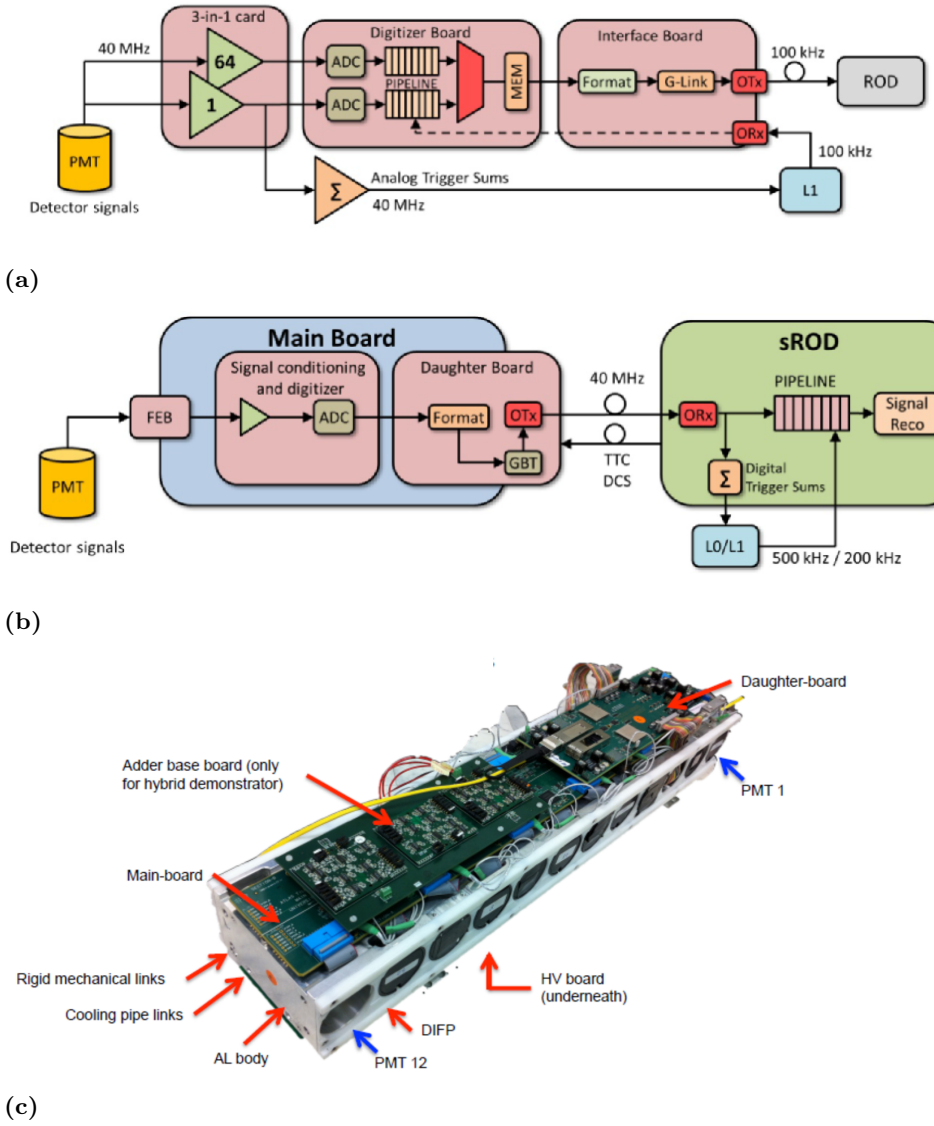


Figure 1: **(a)** Current front-end electronics; **(b)** Equivalent electronics for Phase-II upgrade; **(c)** A single mini-drawer, recently built at CERN for the upgrade of the TileCal electronics.

design, each super-drawer is divided into 4 mini-drawers. One mini-drawer hosts 12 PMTs and 1 daughter board. Each daughter board has one link to the Tile Pre-Processor (TilePPr), thereby reducing potential failure rate by 25% with respect to ATLAS. There are up to 48 PMTs in one super-drawer, in groups of 6 in a digitizer board. There are 16 digitizers for one super-drawer, interfaced by 1 interface card. It is envisaged that the future electronics will have:

- a Tile Pre-Processor (TilePPr), capable of receiving data at 40 MHz as opposed to the current Read-Out Driver (ROD) which only handles 100 kHz,
- an increase in the number of point-to-point links with the front-end electronics,
- improved radiation tolerance,
- a higher read-out bandwidth due to the need to read-out all sampled data to avoid corruption in the front-end pipeline memories.

An evaluation of this new proposed architecture is currently being carried out in the demonstrator project, where a small fraction of the detector (1/256) will be evaluated in test beams and inserted into ATLAS at the next shutdown of the LHC. In the LHC Phase II upgrade, the current Mobile Drawer Integrity ChecKing (MobiDICK) system [4, 5] test-bench will be replaced by the next generation test-bench for the TileCal super-drawers, the new PROMETEO (A Portable Read-Out ModulE for Tilecal ElectrOnics). The MobiDICK system faces challenges against ageing and new technologies [6]. The PROMETEO system is designed to certificate the TileCal front-end electronics by performing multiple tests. The PROMETEO's prototype is being assembled and designed by the University of the Witwatersrand and installed at CERN to gain system experience.

2. PROMETEO (new test-bench): Hardware design

PROMETEO is inspired by the currently used MobiDICK test-bench whose main board is a Xilinx ML507 evaluation board with a Virtex-5 FPGA. The MobiDICK test-bench has a server running on Power PC, which connects to the client via ethernet. It records digital data at a maximum rate of 100 kHz. It uses "slow" canbus to control the current integrator circuit and the HV applied to every PMT and a custom designed ADC board to sample the analogue signals.

PROMETEO has been designed to have the ability to: read-out all channels at the LHC bunch crossing frequency, assess the quality of data in real-time, diagnose malfunctions in each mini-drawer be self-contained and portable for maintenance inside the detector, and be low-cost and scalable for network usage. In the current design being deployed for the hybrid demonstrator that will also have analogue output, PROMETEO will make use of an ADC board. The current version is using a Xilinx VC707 board. Figure 2 shows a block diagram of the PROMETEO.

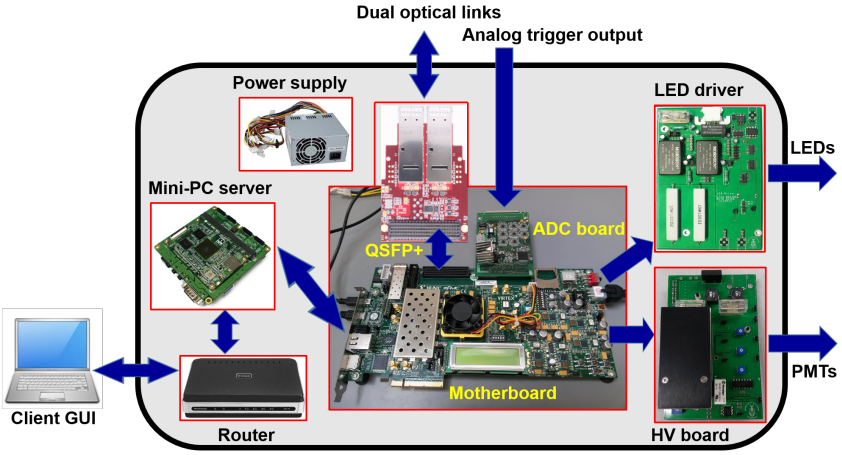


Figure 2: Block diagram of the PROMETEO system.

The PROMETEO system consists of several parts as follows:

- Main board: Xilinx VC707, Virtex-7 FPGA chip, 1 GB DDR3 RAM, two FMC connectors, received through SFP on the mainboard,
- Dual QSFP+ FMC card for digital communication with 2 mini-drawers,
- Analogue to Digital Converter (ADC) FMC card: for the digitization of the analog trigger output from the the hybrid demonstrator adder cards,
- High Voltage (HV) board: to turn on/off the HV and provide the -830 V voltage to power on the photo-multipliers (PMTs),
- Light Emitting Diode (LED) board: to illuminate the PMTs,

- Commercial ATX power supply,
- Mini-PC server: to provide direct connection to the test results when a user logs onto the webpage. It is a low-cost Cortex-A9 ARM processor board based on the Freescale i.MX6 family of System on Chips (SoCs). The mini-PC server uses a Linux, ROOT and Apache environment to host the PROMETEO webpage.
- Ethernet router,
- Aluminum enclosure: whose dimensions are 50 cm × 35 cm × 20 cm in terms of length, width and depth, thickness of 3 mm and weight of 8 kg.

3. PROMETEO: Software design

The software design of PROMETEO is based on direct hardware access technology for FPGAs with direct ethernet connection. Figure 3 shows a block diagram of the PROMETEO system software structure. An IPbus [7] ip-core module on the FPGA that enables direct communication

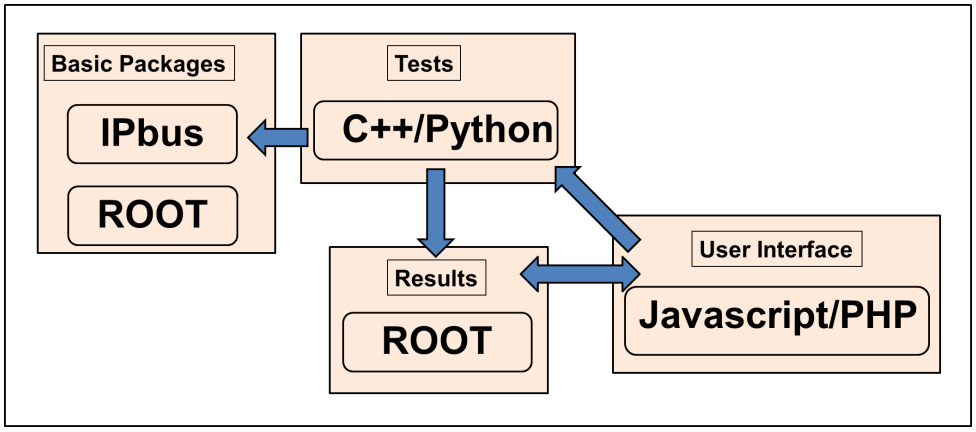
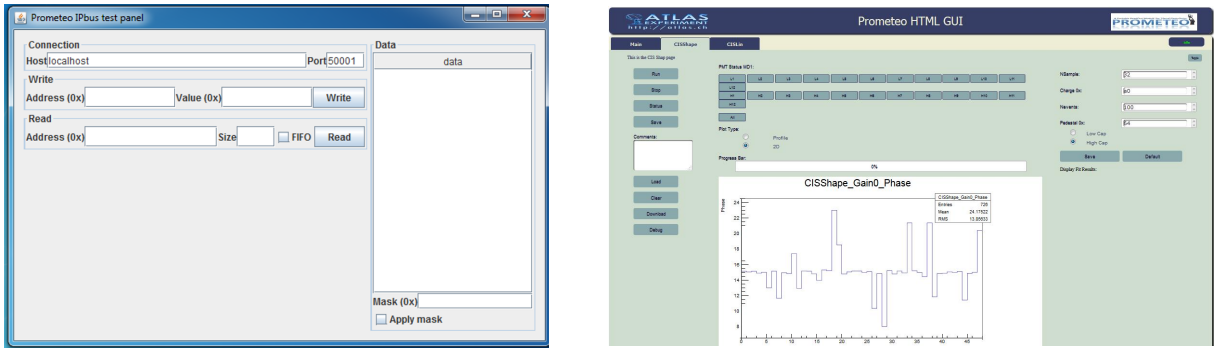


Figure 3: Block diagram of the PROMETEO system software structure.

of the registers is employed. A custom built software version of the IPbus client that is implemented in C++, Java and Python is used to allow multiple developments and tests to perform in parallel. At this stage there are two implementations of the software being developed, namely, one in pure Java and another one in C++/Python. The Java software is inspired by the one in the MobiDICK GUI where a core window loads different tests as plugin tabs, and each one executes and displays a different test. The C++ one implements the tests directly as command line applications. A front-end HTML/Python interface is used to execute the tests and assess the results. Figure 4 shows snapshots of the Java and HTML GUIs used by the client to execute the PROMETEO system tests.

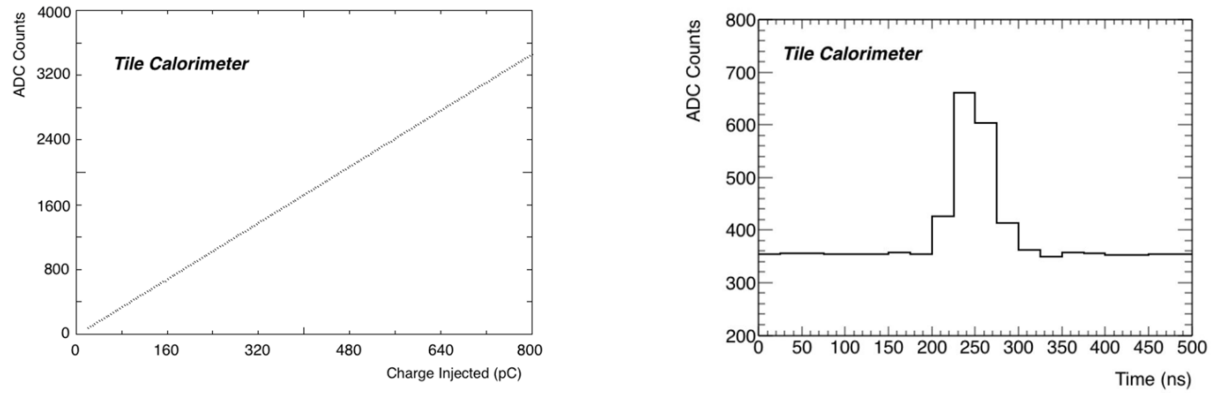
Calibration methods are generally employed in order to assess the performance of the TileCal Demonstrator electronics using the PROMETEO, namely:

- **Charge Injection System (CIS)**: Here, the electronics is tested directly through the injection of a known charge into the front-end boards, thereby simulating a PMT signal. Figure 5a shows a typical result of such a measurement. One can see a good linearity in the Demonstrator's High- and Low-Gain fast readout channels.
- **LASER calibration system**: LASER pulses of known intensity are sent to the PMTs and the PMT response is used to calibrate their gain as well as settings of the trigger timing. A typical response of the PMTs in the new Demonstrator system is shown in Fig. 5b.



(a) **(b)**

Figure 4: Java **(a)** and HTML **(b)** GUIs used by the client to execute the PROMETEO system tests



(a) **(b)**

Figure 5: Results for calibration of the Demonstrator using two methods: **(a)** electronics response to a known charge; **(b)** a triggered LASER pulse. [9]

These results are used for diagnosis of faulty PMTs, 3 in 1 cards, mainboards, daughter boards, optical links and analogue cards. Most of the tests are implemented in the HTML interface, thereby leaving Java as an excellent tool for debugging at expert level.

4. Conclusions

PROMETEO, the next generation test-bench for the certification of the new TileCal electronics has been designed and manufactured in South Africa, in preparation for the LHC phase-II upgrade. PROMETEO is inspired by the current MobiDICK test-bench. It is capable of performing multiple tests on the electronics modules of the upgraded superdrawers. PROMETEO is currently in a prototyping phase and currently serves a hybrid demonstrator of the future Phase-II electronics. All components of PROMETEO have been manufactured and are undergoing tests as they are added to the system. Further tests are being developed and tested in parallel with the development of the demonstrator. PROMETEO software is well advanced and used everyday to assess the stability of the first demonstrator.

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