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Fully programmable SoC based Ethernet to PCI Express Bridge for an ARM Based High Data Throughput Cluster for the sROD of the Tile Calorimeter of the ATLAS detector

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Abstract :

Big Science projects such as the ATLAS experiment at the Large Hadron Collider at CERN require huge amounts of data to be transferred and processed. General purpose cluster computers are not suitable for the data throughput that is required, instead customised computer systems need to be designed and implemented. This project aims to design and build an Ethernet to PCI Express (PCIe) bridge/ packet manager for such a computer system. This board will be created using a Zynq fully programmable System on Chip (Soc) that uses both an FPGA and an ARM processor on a single chip. For initial prototyping a Zedboard Development kit will be used.This board will be in direct communication with a small cluster of ARM processors nodes through a PCIe backplane. Its roll will be to take in data through high speed Ethernet, modify it for PCIe transport and send it to an available ARM node. Once data is processed by a node it can be send back to the Zynq board for Ethernet transport. This project will be part of the electronics upgrade of the Tile Calorimeter. Later designs will have the entire ARM cluster and bridge on a single mezzanine card that can be attached to the Super Read Out Driver (sROD) of the Tile Calorimeter. It will assist with the processing and formatting of the massive amounts of data being received from the detector.

Award :

no

Level :

MSc

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Paper :

yes

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